LINC - Vol. 15

Assembly and Test Procedures

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LINC Volume 15

Assembly and Test Procedures

Section I

LINC ASSEMBLY AND ADJUSTMENT

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LINC ASSEMBLY AND ADJUSTMENTS

Contents

LINC ASSEMBLY AND ADJUSTMENT

1. Introduction

This document contains a complete set of directions for assembling a LINC computer from the kit, Fig. 1.1, and for the operation of maintenance and adjustment programs. A kit may, in some cases, be received with certain components already assembled. In general such pre-assembly will have been done only to facilitate packing and shipping.

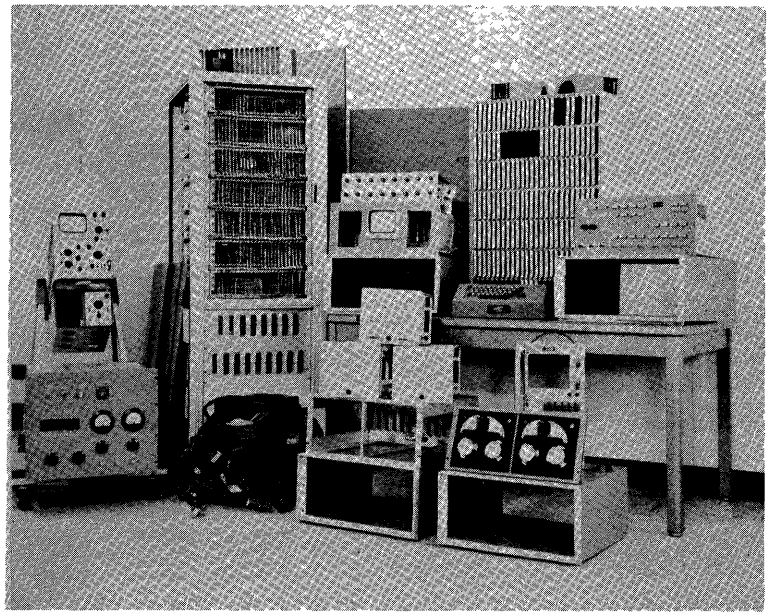

Fig. 1.1

This specification is divided into major sections each of which in turn is broken into steps. The procedures must be followed strictly and one should never proceed beyond a particular step until it is satisfactorily accomplished and understood. Violation of this rule can result in damage to parts of the machine. The need for meticulous care and precise observations cannot be over-emphasized.

The assembly specification has been written with the tacit assumption that all parts of the kit are in working shape as received, i.e., that all that is required is to fit the pieces together and make a few standard adjustments. Much of the writing therefore merely indicates ways to verify that the various parts of the machine are working as they go together. Unfortunately in a device of LINC complexity it will almost invaribly be true at the outset certain of the components will not be in working condition, and therefore certain of the things you will be asked to observe and verify will not at first appear to be true. It is impossible to anticipate all of the difficulties one may encounter, and reference to the Manufacturing Description Volumes 1-12 is required where the indicated procedures cannot be carried out as described herein.

Assembly of a kit requires certain facilities and a limited number of tools. A well-lit working area with a workbench nearby is practically a necessity.

Power for the computer must be available from a grounded, 110 volt, 60 CPS, 3 prong outlet which should be fused at 20 amps. The oscilloscope used in testing should not be plugged into this source.

The assembly description assumes that a Tektronix 561 scope is available. This may come as part of the kit. If not, either a 561 or equivalent must be available. (See Section 2, Parts List Check).

An assortment of screwdrivers, (including some Phillips head type), long nose pliers, clip leads, wire cutters, wire, solder, and a 6 volt soldering iron* should be nearby. In theory most of these should not be required but the occasional error dictates otherwise.

A voltmeter and ohmmeter are required.

Familiarity with pages 1-11 of the Master Wiring Table (Linc Manufacturing Description Vol. 8) and with PROGRAMMING THE LINC (LINC, VOL. 16, PROGRAMMING AND USE) is assumed.

As the procedures described herein near completion, assembly gives way more and more to testing and adjustment. The tests described under the various test and adjustment procedures should be run as the final phase of the assembly operation.

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* A low voltage iron is required in order to avoid the possible hazzard to transistors presented by a regular iron.

The completed Machine is shown in Figure 1.2.

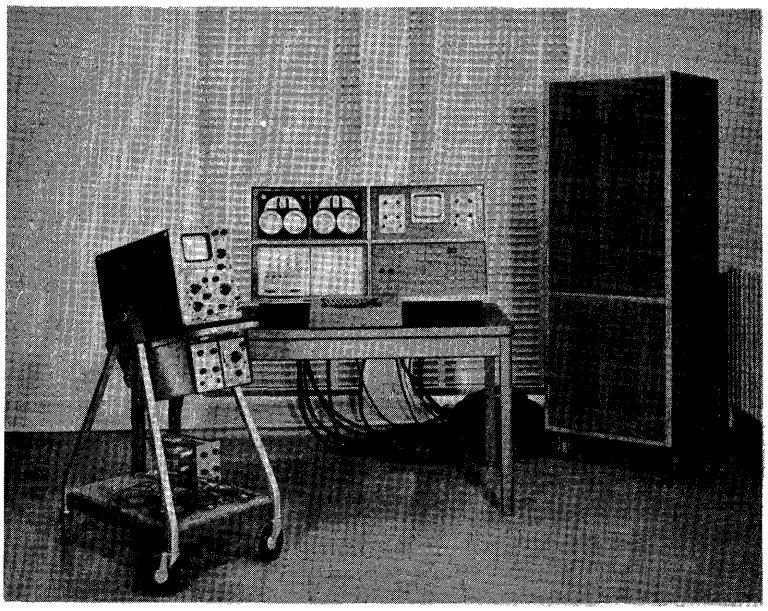


Fig. 1.2

2. Parts Inventory

I. Parts List Check

Verify that you have and can identify the following parts:

1. Documents as follows:

   a) 12 Volumes of LINC Manufacturing Description

   b) LINC Vol. 15 - Assembly and Test Procedures

   c) LINC Vol. 16 - Programming and Use - 1

   d) Tektronix 561 Scope Manual (OPTIONAL) if the 561 Scope is included in the kit. (See Item 17)

2. Wired Cabinet - Including:

2 large louvred doors	2 large side panels
1 small louvred door	2 small side panels

3. Blower Unit - with grill and filter (may already be installed in the cabinet)

4. Power Supply - (May already be installed in the cabinet)

5. Four Control Module Mounting Boxes
(May have the modules already mounted in them - See 7-10 below.)

6. Two Control Module Mounting Pedestals

7. Console Module - Includes:

    1 relay
    5 logic cards, DEC type 1001

8. Scope Module - Includes:

    2 plug-in units
    one with knobs numbered 0 to 3
    the other with knobs numbered 4 to 7 (See also item 17)

9. Tape Transport Module - Includes:

    8 Relays (Also check to be sure that small jumper plug is in place at rear of module. An additional plug, similar to this one, is also included.)

10. Terminal Frame Module - Includes:

    1 Type "A" Blank plug-in unit
    1 Type "B" plug-in unit (The Type "B" plug-in unit includes 6 relays and 2 preamplifier cards.)

11. Memory(s)
    Depending on option chosen:

    A. 2 memory stacks (Standard LINC Configuration)

    or

    B. 1 memory stack and one dummy

12. Memory Fan (Small muffin fan with power cord attached)

13. Keyboard and 8' cable.

14. Nineteen 30' Fantail Cables as listed on Dwg. 1122, Volume 1, Manufacturing Specifications.

15. Set of Logic cards and relays as per Dwg. 1301, Volume 2, Manufacturing Specifications.
    Note that:

    a) 5 of the 1001 cards and 1 relay may already be installed in the console module.

b) 8 of the relays may already be installed in the tape transport module.

c) 6 of the relays and the 2 preamplifier cards may be installed in the Terminal Frame Type "B" plug-in unit.

In addition to the above 1 card extender and 1 card puller should be included.

16. Three empty tape reels
Two loaded tape reels containing virgin tape
Two loaded tape reels labeled Test Programs

17. If you have included the optional 561 in your order, you should also have the following:

a) The basic 561 Scope (modified as per Dwg. 1712, Vol.6, Manufacturing Description), Scope cart, and power cord

b) Tektronix 2B67 Time Base Plug-in-unit

c) Tektronix 2A63 Differential Amplifier Plug-in-unit

d) Tektronix 3A1 Dual Channel Amplifier Plug-in-unit

e) 2 additional LINC scope Plug-in-units identical to those described in item 8 above.

f) 3 direct (i.e. x1) probes type P6028

g) 2 X10 probes type P6006 BNC 9

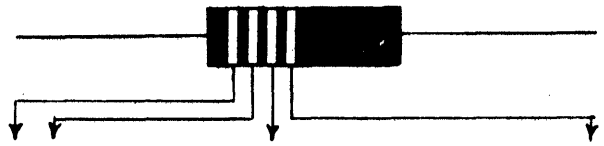
h) a 9 ft. cable as per Dwg. 1719, Vol. 6, Manufacturing Descriptions

i) a BNC - GR connector

18. Accessories - Tape degausser

3. Component Check

Pages 381 thru 383 of the Master Wiring Table (Vol. 8) list the resistors and capacitors that are tied to some of the connectors in the LINC cabinet. Check that the components listed are connected as specified. Correct any errors and remove any unlisted components.



Color Code:

Black	0
Brown	1
Red	2
Orange	3
Yellow	4
Green	5
Blue	6
Violet	7
Grey	8
White	9

Example:

A = Brown
B = Green → $15 \times 10^2 \pm 5\%$
E = Red =1500 $\pm$ 5%
P = Gold =1.5K $\pm$ 5%

4. Power Supply Installation

I. Brief Description of Power Supply*

A. INPUT (male connector on back of supply)

Input source should be 110 VAC, 60CPS, fused for 20A and otherwise unloaded. Supply has its own AC breaker (25A), but this should be reserved for emergencies.

* Trouble-shooting references for this section are:
a. Power Supply Schematic ----- Vol. 1, Dwg. 1208.
b. Cabinet Power Wiring ------- Vol. 8, Pages 12 thru 16.

B. DC OUTPUTS (four multi-pin connectors on top of supply)

SUPPLY	UNLOADED VALUE	PROTECTION	COMMENTS
-18V	-18 ±1	breaker	
-15MC	see comment	breaker	Variable supply. Voltage can be varied from 0V to -25V.
-15V	-17 ±1	breaker	
-10V	-10 ±1	see comment	Supply is current limited.
-3V	0	none	Only a short to the -15V supply will overload it.
+10V	+10 ±1	breaker	
+10MC	see comment	breaker	Variable supply. Voltage can be varied from 0V to +18V.
+18V	+18 ±1	breaker	

All DC outputs (except that of the -3V supply) can be monitored by the meters on the front of the supply. The MC supply voltages are varied by knobs on the front of the supply.

C. AC OUTPUTS (on top and back of power supply)

3 convenience outlets energized at all times and protected in parallel by a 7A fuse. The fuse holder (front of power supply) lights up when fuse is blown.

5 switched AC outlets (female twist-lock connectors) energized only when power supply is on and protected by supply's AC breaker.

II. Equipment Necessary For This Part Of The Assembly

A. LINC power supply (installed in LINC electronics cabinet).

B. LINC AC input cord.

C. LINC remote control cord.

D. LINC console module.

E. Insulated clip lead (approximately 6' long).

F. Voltmeter.

G. Ohmmeter.

III. Installation Of Power Supply

A. Disconnect all cables attached to the power supply.

B. Rough handling of the power supply during shipment may dislodge some of its large storage capacitors. Remove the power supply's front panel and inspect the interior for loose components. Re-anchor any components that need it and remount the front panel.

C. In its off state, the power supply makes no noise. In its on state, it produces a very audible humming noise. Normal on-off operation of the supply is through the ON and OFF pushbuttons on the LINC console. These pushbuttons control a relay (in the supply) that is wired in series with the POWER toggle (front of supply) and hence are operative only when the POWER toggle is in the "on" position. Because of this series connection, power should not come on during any of the following five steps:

1. Turn the POWER toggle to "off".
2. Connect the power supply to its AC source (with the AC input cord).
3. Turn the POWER toggle to "on". Wait about 15 seconds and then turn the POWER toggle to "off".
4. Connect the power supply to the LINC console (with the remote control cord).
5. Turn the POWER toggle to "on".

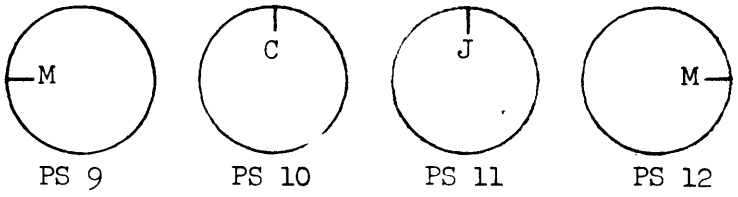
D. Whenever the checkout procedure calls for "power on" or "power off", it should be implemented through the ON and OFF pushbuttons on the console. If any checkout step indicates something wrong, turn power off immediately. This can be done at the console or by throwing the POWER toggle to "off".

1. Flip each circuit breaker switch (front of supply) a couple of times and leave it in the "on" position.
2. Power on.
3. Check that the pilot light (front of supply) is on. Check that the fan (back of supply) is going.
4. Power off.

E. All DC supply voltages (except from the -3V supply) can be monitored with the meters on the front of the supply. As long as these voltages read within the limits indicated in the "UNLOADED" column of the table given in part I of this section, they should be assumed correct. Any significant variation should be investigated and repaired before continuing with the checkout.

1. Turn the +10MC and -15MC knobs clockwise as far as they will go.
2. Power on.
3. Using the meters on the front of the supply, check that the voltage of each DC supply (except the -3V supply) is an appropriate unloaded value. The +10MC and -15MC supplies should read about +18V and -25V, respectively. Check that the MC voltages are variable all the way to zero volts.
4. Power off.

F. The four DC outlets on top of the supply are keyed so that the wrong cables cannot be connected. Check that they are keyed as shown below. Check that the connectors on the mating cables are similarly keyed. (Letters indicate the pin nearest the key):



(viewed from back of power supply)

G. A wiring error in any of the cabinet's power wiring may cause the power supply to malfunction (blow a breaker, for example). If the DC power cables are connected one at a time and power is turned on after each connection, any trouble that develops can be related to the last cable connected.

1. Connect cable PS9 to socket PS9 on top of the power supply.
2. Power on. Wait about 15 seconds or more.
3. Power off.
4. Repeat the above for cables PS10, PS11, and PS12.

H. Operation of the DC circuit breakers can be tested by intentionally shorting each supply to ground. Should a breaker chatter, hesitate a few seconds, or not throw at all, it is faulty and should be replaced.

Prolonged shorting of a supply may damage both the supply and the connecting wiring if the supply's breaker is faulty. Do not, therefore, short any supply for intervals of more than 4 or 5 seconds. This is sufficient time for checking the operation of a breaker.

The following steps test only the DC breakers. It is recommended that the AC breaker not be tested as there is some personal risk involved if it is not done properly. If the AC input source is fused

for 20A as suggested, there is really no need to test the breaker.

1. Put the three toggles on box U in the up position. Put the two toggles on box Z in the down position.
2. Power off (if it is on).
3. Connect one end of an insulated clip lead to Z7so.
4. Power on. Wait about 10 seconds.
5. Press the other end of the clip lead firmly against a nearby ground lug. The -18V breaker should throw immediately.
6. Repeat steps 2 thru 5 for each of the other DC lines with breakers. The appropriate shorting points for each breaker are listed below.

BREAKER	SHORTING POINT
-15V	Z1C
-15MC	U1C
+10V	Z1A
+10MC	U1A
+18V	V17so

I. Mounted above the power supply's front panel is the cabinet's blower. Plug the blower into one of the convenience outlets on top of the power supply.

1. Power on. Blower should come on.
2. Power off. Blower should go off.

5. Power Wiring Check

I. Power Wiring

The LINC cabinet has already undergone an extensive wiring checkout if it has been wired according to specification. In theory this checkout is exhaustive. In practice a mistake or two sometimes gets through due to pilot error. Any wiring mistake will impair the operation of the

machine until it is found and corrected. Mistakes in the power wiring, however, will also tend to cause damage. This section of the LINC assembly procedure provides a cursory but intelligent check of the power wiring. It is very unlikely that a wiring mistake will get past both this and the previous wiring check.

A voltmeter should be used for the following voltage checks, an ohmmeter for the continuity checks.

II. Procedure

A. Pins A, B, and C on every mounting box connector are power pins. The voltage they carry is controlled by the three toggle switches on the front of each box and is summarized below.

PIN	TOGGLE	CONNECTION WITH TOGGLE DOWN	CONNECTION WITH TOGGLE UP
A	upper	+10V supply	+10MC supply
B	middle	+10V supply	+10MC supply
C* (some)	lower	-15V supply	-15MC supply
C* (all others)	------	-15V supply	-15V supply

* See page 380 of the Master Wiring Table.

1. Power off. Put the toggles on every box in the up position.
2. Power on. Adjust the +10MC supply to read +15V.
   Adjust the -15MC supply to read -25V.
3. Check that pins A and B on connector 25 of every box read +15V.
4. Check that pin C on each of the following connectors read -25V: K25, L25, M25, N25, P25, R25, T6, U1, V25.
5. Check that pin C on each of the following connectors reads about -17V:

   K24, L24, M23, N18, P20, R19, S25, T25, U25, V20, W25, X25, Y25.
6. Power off. Put the toggles on every box in the down position. Power on.

7. Check that pins A and B on connector 25 of every box read about +10V.

8. Check that pin C on connector 25 of every box reads about -17V. Check that pins T6C and U1C read about -17V.

9. Power off.

B. The voltage carried by all other power pins never varies.

1. Power on.

2. Check that the following terminals read about -18V: T20S, T23S, Z2F, Z2Z, Z7F, FH21, FU31.

3. Check that the following terminals read about -17V: FH16, FL32, FS32.

4. Check that the following terminals read about -10V: V8E.

5. Check that the following terminals read about +10V: FJ30.

6. Check that the following terminals read about +18V: T25Z, V16S, FH5.

7. Power off.

8. Check that there is continuity between Z5so and the following terminals: T20X, T23R, Z11D, Z18D, FH1, FH17, FH20, FJ1, FL17, FS1, FS2, FT1, FT17, FU1.

9. Check that there is no continuity between the following pairs: Z11M and Z11N, Z12M and Z12N.

6. Insertion of Circuit Cards

Drawings 1034 and 1035 (Vol. 12) specify the type of circuit card (called PIU type on the Dwg.) to be inserted in each cabinet connector. Using these drawings as a guide, insert all of the cabinet's circuit cards. Do not insert the memory plug-in units.

The circuit cards are polarized to prevent improper insertion. You must, however, be careful to seat them properly. After insertion, make an independent check of the correctness of circuit card type number in each position. This step is extremely important.

7. Logic Checkout, Phase I - Basic Pulses

A. Preliminary Preparations

1. Make sure all front-back cables are connected.
2. Make sure all toggle switches on the cabinet's mounting boxes are in the down position.
3. Check that five 1001's are inserted in the slots in the console module.
4. Install the six 30' cables which connect the console module to the cabinet. These cables connect the following plugs:

FANTAIL PLUG	CONSOLE PLUG
FL	CA
FM	CB
FP	CC
FN	CD
FR	CE
FS	CF

B. Verification of Master Reset Pulses

Whenever power is turned on or off, a train of master reset pulses should occur. By setting the scope to sweep with internal synchronization, view the master reset pulses at N2W (see Dwg. 1007, Vol. 12). A train of pulses should appear whenever the power is turned on or off. Note that the pulse amplitude builds up upon power turn-on

(as the -15 volt supply comes up) and diminishes upon power shut-off.

These pulses should always result in the following console lights being off immediately after power is turned on:

1. All lights in the INSTRUCTION (C) register.
2. All pushbutton lights except the power "ON" switch.
3. The RUN and PAUSE lights.
4. The RELAY register lights.

The remaining lights on the console; namely the accumulator, LINK, MEMORY CONTENTS register, MEMORY ADDRESS register, and INSTRUCTION LOCATION register lights will come on randomly.

C. Verification of the Clear and Auto Restart Pushbuttons and the Stop Lever.

With power on, press the CLEAR button. The light on this button will come on. Twist the DELAY knob and vernier to their most clockwise positions. Press the AUTO RESTART pushbutton. Observe the counting that takes place in the MEMORY ADDRESS register (S register). Vary the speed of the counting by varying the DELAY knob setting. Verify that the S register counts up to its full capacity (3777_8) and then repeats, starting at 0.

Now depress the STOP lever. This will turn off the CLEAR and AUTO RESTART lights and stop the counting in the S register. In fact this lever will always have the same effect on the console lights that the master reset pulses (see above) have.

D. Verification of the Fill Pushbutton and the Left and Right Switches.

Raise all toggles of the LEFT and RIGHT SWITCHES. Press the FILL pushbutton but do not release. The FILL light will remain on as long as you hold your finger on the button. All lights in the MEMORY CONTENTS (B) and (S) register will be on. Releasing the button will turn off the FILL light and turn on the EXAM light. The S register lights should remain on but, with no memory in place, some of the B register lights may go off.

Now place all LEFT and RIGHT SWITCHES in the down (i.e., "0") position. Press FILL, which should turn off all lights in B and S. The FILL light will once again remain on so long as you hold the button down. Releasing it shuts off the FILL light and turns on the EXAM light. The S register lights should remain off; the B register lights will go to an arbitrary state.

Now that this much of the LINC is operating we are ready to proceed with installation of the memory.

8. Memory Installation and Tuning

I. Installation

A. The LINC memory consists of two plug-in units. One memory plug-in unit is to be inserted in connectors Z1 - Z5, and the other unit is to be inserted in connectors Z6-Z10. After insertion, the cutouts in the backplates should form a circle (see Dwg. 1407). To effect this, one unit's backplate must be rotated 180^{0} before the unit is inserted.

1. Unscrew backplate of the unit and rotate it so that the cutout faces the opposite direction. Note that the backplate's screw holes are only countersunk on one side of the plate, so make sure the backplate is not reversed in the process.

2. Insert the memory plug-in unit in connectors Z1-Z5. Be forewarned that it requires a considerable amount of muscle power to get the unit inserted all the way. You can determine whether or not you've got it inserted all the way by viewing it from the wiring side of Z box.

3. Insert the second unit in connectors Z6 - Z10.

B. The memory's cooling unit is a ROTRON whisper fan that attaches to the backplates of the plug-in units (see Dwg. 1407). Before the fan can be attached, it has to be equipped with a cord and connector.

1. Attach a 2 ft. twin lead cord (#18 AWG or heavier) to the whisper fan. Attach a HUBBEL 7428 connector to the other end of the cord.

2. Mount fan on back of the two plug-in units as shown in Dwg. 1407. Fan is to be attached so that air flow will be into the plug-in units. (Air flow direction is indicated by an arrow on one side of the fan.)

3. Plug fan cord into socket on top of the supply.

4. Power on. Fan should come on.

5. Power off. Fan should go off.

II. Tuning

A. Located on the right-hand side of the power supply (when viewed from the front) is a small hole. This hole provides access to the adjustment screw for the -3V supply. The adjustment screw for the -18V supply is located on the front of the power supply.

1. Put the upper toggle on Y box in the "up" position. Check that all other mounting box toggles are in the "down" position.

2. Power on. Adjust the +10MC supply to read +5V.

3. Adjust the -18V supply to read -18V.

4. Using a voltmeter, check that pins Z16E and Z19F read -3V. If they don't, adjust the -3V supply until they do.

B. Memory timing is controlled by two delays called MDEL 1 and MDEL 2. The circuits used for these have to be adjusted to give delays of appropriate duration. The adjustment requires the use of a scope.

Set the scope to trigger externally on a negative slope. Set the scope's time base for a sweep rate of 1/2 μsec/cm.

1. Power on. Push the CLEAR button on the console. Push the AUTO RESTART button and turn both DELAY controls counter-clockwise all the way.

2. Attach the scope's probe to R4J and adjust the triggering until the following waveform appears: (Trigger on M6P, negative slope.)

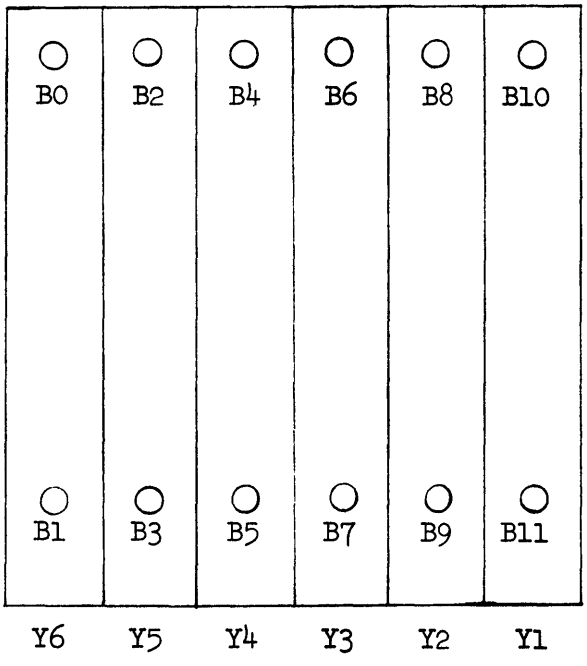
3. The circuit card plugged into R4 has an adjustment hole in the back. This hole gives access to the trim pot that controls the duration of delay MDEL 1. Using a screwdriver, adjust the delay (negative part of display) to 1.1 μsec.

4. Move the probe to R5J and adjust the scope's triggering until a waveform similar to the previous one appears. This is MDEL 2. Adjust MDEL 2 (via the trim pot in R5) to 1.8 μsec. (Trigger on R4J, negative slope.)

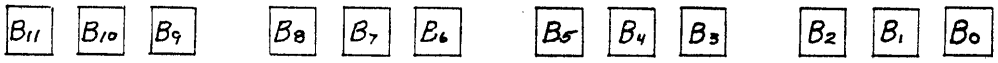
5. Disconnect scope.

C. Associated with each bit of the MEMORY CONTENTS register is a memory sense amplifier. These amplifiers identify the information coming from memory and transfer it into the MEMORY CONTENTS register. In order to do this, the amplifiers have to be adjusted properly.

The memory sense amplifiers are mounted on the cards plugged into Y1 thru Y6. Holes in the back of these cards provide access to trimpots that adjust the amplifiers. The drawing below indicates which bit (B) of the MEMORY CONTENTS register is affected by each adjustment hole. Label the holes on your cards so that they can be easily identified during the adjustment procedure.



Label also the lights of the MEMORY CONTENTS register. This is easiest done by putting a strip of tape above the lights and writing on that. The diagram below shows the proper label for each light.



D. In the CLEAR mode, LINC writes and then reads each memory register. If it does not read exactly what it wrote, LINC stops and the information read is left in the MEMORY CONTENTS register.

The pattern LINC writes is not the same on each pass through memory. On alternate passes, the pattern 0000_8 is written. On all other passes, the pattern 7777_8 is written. Regardless of the pattern being written, however, the contents of each memory register is always left equal to 0000_8.

In using the CLEAR mode for tuning up memory, a jumper is attached that forces the CLEAR mode to use the pattern 0000_8 on every pass. After memory is tuned, therefore, the contents of the MEMORY CONTENTS register should always be 0000_8, that is, its lights should always be extinguished.

1. Jumper Z20V to gnd.

2. Press STOP. Then push CLEAR and AUTO RESTART. Turn the DELAY gross control all the way clockwise (position 4) and the DELAY vernier all the way counter-clockwise.

3. If the lights in the MEMORY CONTENTS register appear permanently extinguished, proceed to step 4. If any light is on or flickering, adjust the corresponding sense amplifier (turn counter-clockwise) until the light just extinguishes and continue turning another full turn.

   NOTE: A light corresponding to a previously adjusted sense amplifier may begin to flicker again during the adjustment of another sense amplifier. If this happens, simply readjust the corresponding sense amplifier.

4. Adjust the sense amplifier for bit zero (turn clockwise) until the corresponding light begins to light up. Then turn the trimpot (counter-clockwise) until the light just extinguishes and continue turning another half turn. Adjust all other bits of the MEMORY CONTENTS register in exactly the same way.

5. Remove the jumper between Z20V and gnd.

6. Adjust the +10MC supply to +10V.

E. To find the operating margins for which the sense amplifiers are now tuned, we vary the +10MC supply until the CLEAR mode begins to detect errors (lights begin to noticeably flicker). Since the jumper has been removed, both patterns are again being written. When the +10MC supply is varied toward +5V, a light coming on indicates an error (a bit "picked up"). When the +10MC supply is varied toward +15V, a light extinguishing indicates an error (a bit "dropped").

Varying the +10MC supply has the effect of varying the size of the signal seen by the sense amplifiers. The range over which we can vary it without the CLEAR mode's detecting an error is therefore a measure of the sense amplifier operating margins. The memory system can be considered acceptably adjusted if the +10MC supply can be varied between +6V and +14V without errors occurring.

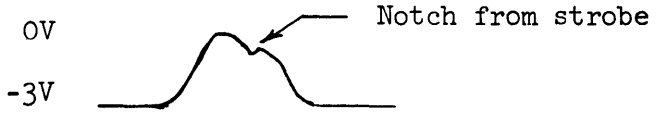
1. Very slowly, adjust the +10MC supply toward +5V and note the voltage at which the CLEAR mode begins to detect errors.

2. Adjust the +10MC supply toward +15V and note the voltage at which the CLEAR mode begins to detect errors.

F. The adjustment of MDEL 1 was only approximate as the proper adjustment varies from machine to machine. For its final adjustment, we again need a scope.

1. Adjust the +10MC supply to +12.5V.

2. Attach the scope probe to Y1K. Trigger externally on M6P (negative slope). Adjust triggering until the following waveform appears.



3. There is a definite notch in the top of the positive pulse. The position of this notch is controlled by MDEL 1. If MDEL 1 is properly adjusted, the notch will lie in the middle of the pulse. If it does not, adjust MDEL 1 until it does.

4. Repeat section D. The operating range should now be the same or better than before.

5. Adjust the +10MC supply to +10V. Put the upper toggle on Y box in the "down" position.

9. Logic Checkout, Phase II - Console Functions

A. Filling and Examining.

Clear the memory. Press STOP. Set all LEFT and RIGHT SWITCHES down. Press EXAM. The EXAM light should come on and remain on. The B and S register lights should all be off. Depress the STEP EXAM lever once. The S register will step to select memory location 1. Depress it several more times and observe that the S register counts once for each depression. The EXAM light will remain on and all of the B register lights will remain off. Set the DELAY knob to slowest speed (most clockwise) and press AUTO RESTART. The S register will count and as it does so, successive addresses in the memory are examined and their contents placed in the B register. Because the memory was cleared initially, no "1"'s should appear in B.

Now place all of the LEFT SWITCHES in the "up" position and press EXAM. The AUTO RESTART light will go off and the S register is set to the all ones value specified in the LEFT SWITCHES. Press the STEP EXAM lever once and observe that S counts from all ones to all zeros (i.e., $3777_8 \rightarrow 0_8$).

Now raise all the RIGHT SWITCHES (leaving the LEFT SWITCHES up also). Press the FILL button. It will react as above, proceeding to EXAM when released. Now that the memory is in place, however, the B register lights, following the release should have meaning, and as the memory location (3777) has just been filled, the lights should all be on.

Raise and continue to hold up the FILL STEP lever. The FILL light will come on and the EXAM light go off. All B and S lights will be lit. Now release the lever. The FILL light goes off and the EXAM light comes on. All B and S lights go off. Raise the FILL STEP lever again. Everything but the S register behaves as before. This time the S register lights stay off until the lever is released at which point it counts to 1. Repeat this process and observe that each time upon raising the lever, (1) the S register remains unchanged; (2) the B register lights all come on; (3) the FILL light comes on, while upon releasing the lever, (1) the S register counts up by one, (2) the B register lights go off and (3) the EXAM light comes on in place of the FILL light.

After thus having filled a number of registers with "all ones", set the LEFT SWITCHES all down and press EXAM, thereby examining

register "0" where "all ones" have recently been stored. Verify that these ones appear in the B register. Now, using repeated depressions of STEP EXAM, examine successively the registers which were filled in the above process. When the boundary is crossed between those registers that were filled with "ones" to those that had not been filled, the B register lights will go off and will remain off as further registers are examined.

Using the EXAM, FILL, STEP-EXAM, and FILL-STEP switches in conjunction with the LEFT and RIGHT SWITCHES, practice filling small sections of memory with sets of arbitrary numbers.

B. START Pushbuttons.

Clear the memory. Push the "START 400" pushbutton. P should contain 400_8, the C register cleared, and the I CYCLE light on. Press "START 20". The only change should be that P should now contain 20_8. Press "START RS". The contents of the rightmost 10_{10} bits of the RIGHT SWITCHES should appear in P. Repeat this for various values of the RIGHT SWITCHES.

Note that none of the start buttons lights up when pressed.

C. INSTRUCTION-BY-INSTRUCTION, CYCLE-BY-CYCLE and STEP.

Enter a JMP 20 (6020_8) instruction into memory register 20 from the switches. Press START 20. Verify that the RUN light is on. Press the INSTRUCTION-BY-INSTRUCTION button whose light will then come on. Verify the following lights:

RUN - off

CYCLE - I light on

B and C registers - 6020_8

P and S registers - 0020

Raise the RESUME lever. The INSTRUCTION-BY-INSTRUCTION light will go off and the RUN light will come back on. Depress the STEP lever. The INSTRUCTION-BY-INSTRUCTION light will come on again and the RUN light will go off.

Now press CYCLE-BY-CYCLE which should turn on its light and shut off the INSTRUCTION-BY-INSTRUCTION light. Press STEP a few times and note that the machine steps from the I CYCLE to the 0 CYCLE and back upon successive steps.

Press AUTO RESTART and observe that you can control the rate of the cycle stepping by varying the DELAY knob. Both the AUTO RESTART and CYCLE-BY-CYCLE lights will be on. Shut them both off by pressing STOP.

D. DO Lever, The ACCUMULATOR and RELAY Registers.

Enter a CLR instruction (0011_8) in the LEFT SWITCHES and raise the DO lever. All ACCUMULATOR lights and the LINK light will be turned off. Now enter a COM instruction (0017_8) in the LEFT SWITCHES and DO. This will complement the A register, (but not the LINK BIT) thereby turning on all its lights. A second DO (COM) should shut them all off again, etc.

Leaving all "1"'s in the ACCUMULATOR, enter an ATR instruction (0014_8) in the LEFT SWITCHES and execute it by raising DO. The six RELAY lights should be turned on. Now do a CLR instruction, returning the ACCUMULATOR to all zeros, and then another ATR. This should clear the RELAY lights once again.

Now perform a

LDA i

1

instruction from the switches by entering LDA i (1020_8) in the LEFT SWITCHES and 1 (0001_8) in the RIGHT SWITCHES and raising DO. This should enter a 1 into A_0, the rightmost bit of A. Next enter a ROL 1 instruction (0241_8) in LEFT SWITCHES and by successive DO's, verify that the bit rotates around the A register. Now DO a ROL i 1 (0261_8) and verify that the one rotates through the LINK BIT as well.

E. Miscellaneous.

1. Enter a JMP 1777 (7777_8) into the LS and DO. All C and P register lights should be lit.

2. Execute a SET 2 instruction CYCLE-BY-CYCLE from the switches
3
(holding the CYCLE-BY-CYCLE button down, raise the DO lever). Step from the I CYCLE successively to the X, O, and E CYCLES by successive pressings of the STEP lever.

10. Logic Checkout, Phase III - SIMPLE PROGRAMS

This section involves verification of the ability to run the programs required for the Ladder Adjustment in Section 10. These programs employ the following instructions:

JMP

RSW

ADA (i=1, β=0)

STA (i=0, β=0)

SET (i=1)

XSK

The JMP instruction has already been exercised to some extent in Section 9 above. The other instructions should now be verified.

STEP 1

Place an RSW (0516_8) instruction in the LEFT SWITCHES, and raise and release the DO lever. This action should place the number contained in the RIGHT SWITCHES into the ACCUMULATOR. Repeat this for various settings of the RIGHT SWITCHES and verify that in every case the number appears properly in A.

STEP 2

Now set up the following two order programs in the memory using the FILL and EXAM features discussed in Section 8.

Memory Location	Instruction	Octal Equivalent
20	RSW	0516
21	JMP 20	6020

Press start 20. The program should run. By changing the contents of the RIGHT SWITCHES as the program is running, you will be able to change the ACCUMULATOR contents. The ACCUMULATOR lights should follow the numbers you enter in the RIGHT SWITCHES. Verify that this is true for each pattern you enter in the RIGHT SWITCHES.

STEP 3

Using the RSW instruction, place the number 5252_8 in the ACCUMULATOR. Place an STA instruction (1040_8) in the LEFT SWITCHES and any arbitrary number (N) between 0 and 3777_8 in the RIGHT SWITCHES. Raise the DO lever. Record the number N on a slip of paper. Repeat this for several values of N (include at least the values 0, 1777, 2000, 3777). Now examine the memory locations specified by the various N's you have used. Each of these locations should have the number 5252_8 stored in it.

STEP 4

Set up the following program in the memory:

Location	Instruction	Octal
20	RSW	0516
21	STA	1040
22	400	0400
23	HLT	0000

This program reads the contents of the RIGHT SWITCHES into the ACCUMULATOR, stores this number in location 400, and then halts. Press start 20 and verify that it works. Verify further that it works for any number that you enter in the RIGHT SWITCHES and for any memory location ($0-3777_8$) which you specify in location 22, (i.e., try numbers other than 400 in location 22).

STEP 5

Set up the following program in the memory:

Location	Instruction	Octal
20	ADA i	1120
21	1	0001
22	JMP 20	6020

Run the program at slow speed in the I-STOP mode by:

1. Pressing START 20.
2. Entering a 20 into the LEFT SWITCHES.
3. Pressing I-STOP (Program should stop at 20).
4. Pressing AUTO RESTART.
5. Adjusting the DELAY knob coarse control fully clockwise.

This program should count in the ACCUMULATOR. Adjust the DELAY vernier knob so that you can observe the counting. Be sure that the end-around-carry works properly. To do this you may want to step manually through the last few counts before the ACCUMULATOR is full of "1's". Raising the (RESUME lever will turn off AUTO RESTART (but not I STOP) and so the computer will stop at location 20 (as specified in the LEFT SWITCHES for the I STOP). The next RESUME will run through the loop one more time, adding 1 to the ACCUMULATOR and again stopping at 20. Each raising of RESUME, will cause one more pass through the loop. To resume AUTO RESTART, simply press AUTO RESTART. To resume full speed operation, press STOP (to clear I STOP) and then raise RESUME.

STEP 6

Modify the program of STEP 5 by placing a 400_8 in register 21. Now run the program at slow speed as directed above. Note that counting now takes place only in bits 8-11 of the ACCUMULATOR except that when all these bits are "1's" the next addition causes an end-around-carry which counts into the low order eight bits.

STEP 7

Verify that the SET instruction works for the i=1 case. To do this, put SET i 3 (0063_8) in LEFT SWITCHES and some number N in RIGHT SWITCHES. Raise DO. Now examine register 3 which should contain the number N. Verify that this works for β registers other than 3, and for various N's in the RIGHT SWITCHES.

STEP 8

Verify that the SET instruction (i=1 case) can be executed from memory by using the following program:

Location	Instruction	Octal
20	SET i β	60 + β
21	N	N
22	HLT	0000

Check this for several values of β ($0 \rightarrow 17_8$) and several values of N ($0 \rightarrow 7777_8$).

STEP 9

Now verify the XSK instruction by entering the following program:

Location	Instruction	Octal
20	SET i 2	0062
21	-4	7774
22	XSK i 2	0222
23	JMP 22	6022
24	HLT	0000

Run this program in the INSTRUCTION-BY-INSTRUCTION mode. Hold the INSTRUCTION-BY-INSTRUCTION lever down while pressing START 20, to get started. Then press INSTRUCTION-BY-INSTRUCTION once to execute each instruction. The program should proceed through the following registers: (Watch the P register lights.)

20, 22, 23, 22, 23, 22, 24

Now verify that, at full speed, the program arrives at the HLT properly merely by pressing START 20 without the INSTRUCTION-BY-INSTRUCTION lever.

STEP 10

Set up the following program in the memory:

Location	Instruction	Octal
20	RSW	0516
21	ADA i	1120
22	1	0001
23	ADA i	1120
24	1	0001
25	JMP 20	6020

Run the program in the INSTRUCTION-BY-INSTRUCTION mode. Assure yourself that the program operates correctly for various values of the RIGHT SWITCHES.

11. Ladder Adjustment

A. Adjustment Principle

There are three ladders* in the LINC which convert numbers in the ACCUMULATOR and B register into voltages. Two of the ladders are attached to the ACCUMULATOR and the third to the B register. The two ladders attached to the ACCUMULATOR are known as the "Analog to Digital Ladder" and the "Y Ladder" while the one attached to the B register is known as the "X Ladder". This

* See Dwg. 1027, Vol. 12

terminology derives from the use of the various ladders to provide voltages for:

Analog to Digital (A to D) Conversion

Scope Y - deflection

Scope X - deflection

Potentiometers on the DEC 1561 ladder cards permit adjustment which assures that all steps of the same magnitude result in equal differences in voltage output. Thus changing the number in the register from 37_8 to 40_8, for example, should produce the same change in the output voltage of the ladder as a change from, say, 40 to 41. Note that switching from 40 to 41 switches only the ladder element associated with bit 0, whereas the change from 37 to 40 switches bits 1 through 5 as well.

The adjustment procedure involves starting with the potentiometer for bit 0 set somewhere in mid-range.* Switching the register-contents between the numbers 0 and 1 will then produce some voltage shift, ΔV, at the output of the ladder. This same shift will appear if we alternate between 2 and 3, 4 and 5, 10 and 11, 20 and 21, etc., (Note that in all of these pairs the only change is in bit 0 which switches "0" to "1".).

Thus in each case the change in the ladder output voltage will be ΔV.

Suppose now we step repeatedly through the numbers 1-2-3. The change from 2 to 3 produces the standard ΔV as discussed above. The change from 1 to 2 causes bit 0 to go from a "1" to a "0" and this, by itself contributes an output voltage difference of $-\Delta V$. The object is to adjust the potentiometer for bit 1 so that the change in that bit from "0" to "1" contributes exactly $+2\Delta V$ to the output when properly adjusted. Then the step from 1 to 2 will produce a resultant change at the output of $2\Delta V - \Delta V = \Delta V$, identical to the change in stepping from 2 to 3. Viewing the output on the 561 scope we can make this adjustment.

The next step is to adjust the potentiometer on bit 2 so that it contributes exactly $+4\Delta V$ to the output. Having bits 0 and 1 already set, we step repeatedly through the numbers 3-4-5. The

* See Figure 11.1 for the layout of the potentiometers for each ladder. Unused potentiometers may be set at any arbitrary value but should not be changed during or after adjustment.

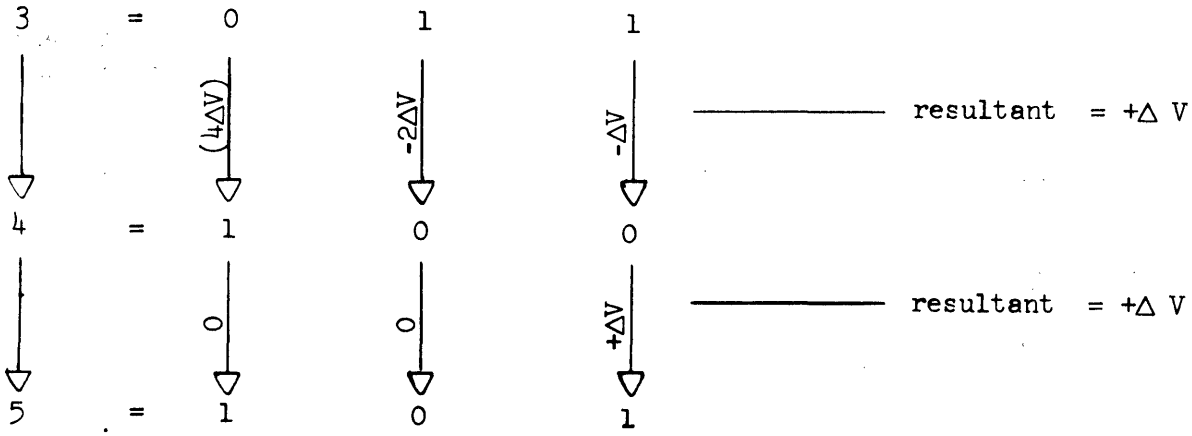
step from 4 to 5 produces an output change of Δv. The step from 3 to 4 switches bit 1 from "1" to "0" (introducing a shift of $-2\Delta V$) and bit 0 from "1" to "0" (introducing a shift of $-\Delta V$). If we adjust the potentiometer on bit 2 so that the resultant overall shift is $+\Delta V$ we must have adjusted that bit to contribute exactly $+4\Delta V$ inasmuch as if

$$X-2\Delta V-1\Delta V = \Delta V$$

then

$$X = 4\Delta V$$

All of this may be diagramatically represented as follows:



The quantity on the arrow is the change in the output due to the change in the particular bit. If we assume that all of the voltages are precise except the $4\Delta V$ in parenthesis, then when the two resultant voltage changes are made equal by adjusting the bit 2 potentiometer, the value contributed by this bit must exactly be the desired $4\Delta V$.

The next stage is adjusted by stepping through the numbers $7\text{-}10_8\text{-}11_8$, and the following one $17_8\text{-}20_8\text{-}21_8$, etc., at each stage adding a new bit, and adjusting the next potentiometer. Once the potentiometer for a given stage is set it must not be changed later in the procedure. If it is, the adjustment must be done over again starting at the first stage.

The ensuing procedures are to be performed in order - that is, the Y ladder adjusted first, the A to D ladder adjusted next, and the X ladder adjusted last.

B. Maintenance Scope Balance

Before attempting any ladder adjustments, balance the 2A63 Differential Amplifier of the 561 Scope as follows:

1. Set both AC-DC-Gnd switches to Gnd. and the volts/div. switch to 1 mvolt.

2. Set the AC Stabilized switch to "on" and using the vertical position knob on the 2A63 position a free-running trace to the horizontal center-line of the scope.

3. Set the AC Stabilized switch to off and adjust the front panel DC Bal control to bring the trace back to the centerline of the graticule.

4. Repeat steps 2 and 3 until the trace remains in the scope center with the AC stabilized switch in either position.*

C. Y Ladder Adjustment

1. Shut off power. Remove the 1561 card in V13 and remount it in that location on an extender card. Turn power on. Adjust all the potentiometers on the card approximately to mid-range.

2. Set up the following program in the memory via the switches:

Location	Instruction	Octal Equivalent
20	RSW	0516
21	ADA i	1120
22	1	0001
23	ADA i	1120
24	1	0001
25	JMP 20	6020

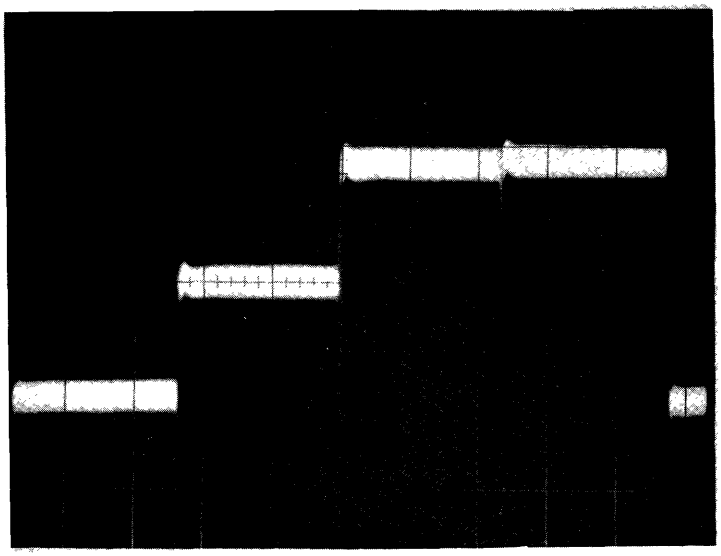
* Adjustment of the front panel DC balance is dependent upon proper adjustment of the internal coarse DC Balance Control. If front panel adjustment cannot be obtained then refer to the 2A63 manual for calibration of the internal coarse DC Balance Control.

3. Plug the 2A63 differential amplifier into the 561 scope and by running the above program, sync the scope sweep on the positive transition of P3T (RSW) via the external trigger. Now set the switch on the (-) input to Gnd and the one on the (+) input to AC. Connect the (+) input to the Y Ladder output at V13F (See Dwg. 1027, Vol. 12) using a direct probe. Set the volts/division to 5mv. and put the "AC Stabilized" switch off. Set the time base for .5 ms./division.

4. Set the coarse control on the computer's DELAY knob to position 2, and run the program in the INSTRUCTION-BY-INSTRUCTION mode with AUTO-RESTART.

5. Set the number 0001 in the RIGHT SWITCHES.

6. You should now be able to obtain a trace on the 561 scope showing the output voltages resulting from stepping the ACCUMULATOR repeatedly through the numbers 1-2-3. By adjusting the DELAY knob it should be possible to produce a picture showing just one complete cycle,* as follows:



These steps are the output voltages resulting from stepping through the numbers 1-2-3. Be sure that the step of double length duration (due to the additional instruction at that point in the loop) is the 3rd step of the sweep (adjust the trigger lever for this). Then adjust the appropriate potentiometer so that the successive steps are equal in size and in ascending order.

* Do not attempt to do this except with the .5 ms/division sweep rate.

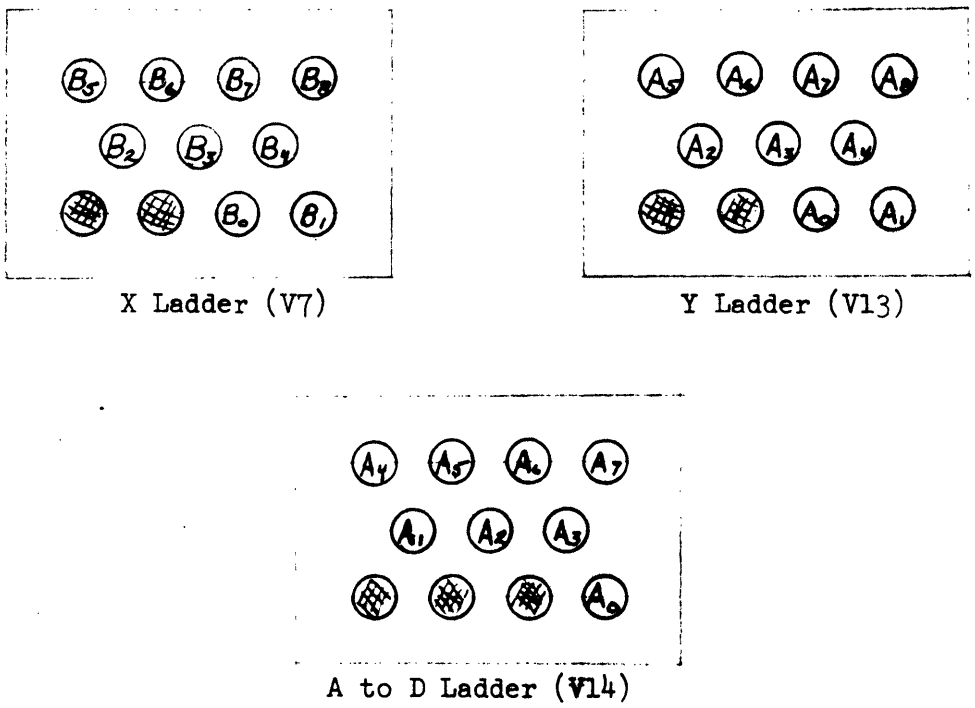


Fig. 11.1

7. Adjust the potentiometer for A_1 (See Fig. 11.1) so that the heights of the two steps are just equal. In order to do this, first adjust the potentiometer so that the steps are in the proper (ascending) order and of approximately the same height. Then desynchronize the scope temporarily by speeding the sweep rate to 20 μs/cm and setting the triggering level knob to the free run position. Three horizontal lines will appear. Adjust the A_1 potentiometer so that these lines are equally spaced. It is vitally important after adjusting each potentiometer to resynchronize the scope (turning the sweep rate back to .5 ms/division and readjusting the triggering level) in order to verify that the three steps are still in the proper order before proceeding to the next stage.

8. Repeat steps 5 through 7 for all successive stages, in turn using the following table:

Number (octal) in RIGHT SWITCHES	Potentiometer to Be Adjusted
0001	A_1
0003	A_2
0007	A_3
0017	A_4
0037	A_5
0077	A_6
0177	A_7
7776	A_8

(Note the non-conformity of the last stage resulting from the fact that in the Y ladder (i.e., for the Y scope deflection) bit 8 is used as a sign bit so that the value 0000 corresponds to the middle of the scope, 377 to the top, and 400 to the bottom.)

D. Analog-To-Digital Ladder Adjustment

Adjustment of the A to D ladder is similar to the adjustment of the Y ladder. The 1561 at V14 should be placed on the extender, and the scope probe placed on V14F. The same program is used as for the Y ladder adjustment and run in the same INSTRUCTION-BY-INSTRUCTION mode.

Note in Fig. 1 that the potentiometers for the bits differ from those of the Y ladder by one position since there are only 8 bits in the A to D conversion as opposed to 9 bits for scope deflection.

The numbers which should be entered in the RIGHT SWITCHES and the corresponding potentiometer to be adjusted are as follows:

RIGHT SWITCHES	Potentiometer
0001	A_1
0003	A_2
0007	A_3
0017	A_4
0037	A_5
0077	A_6
7776	A_7

Follow the same procedures outlined in the Y ladder adjustment.

E. X Ladder Adjustment

1. Mount the 1561 card in location V7 on an extender and turn on power. Adjust all of the potentiometers on the card approximately to mid-range.

2. Set up the following program in memory:

Location	Instruction	Octal Equivalent
20	RSW	0516
21	STA	1040
22	26	0026
23	ADA i	1120
24	400	0400
25	SET i 2	0062
26	( )	----
27	XSK i 2	0222
30	XSK i 2	0222
31	JMP 20	6020

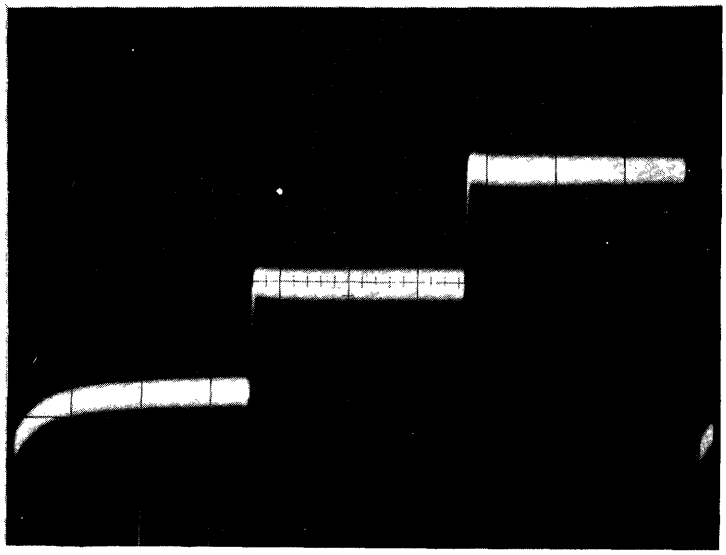
3. Put the number 0001 in RIGHT SWITCHES, and START 20.

4. Using the 2A63 differential amplifier in the 561, synchronize the scope sweep on the positive transition of P2S (SET) via the external trigger. Set both the (+) and (-) input switches to DC. Connect the (+) input to V7F and the (-) input to V13F using direct probes on both. Set the volts/division to 5 mv. and the time base for .5 ms/division. Set the AC Stabilized switch to on.

5. Put the number 0002 in LEFT SWITCHES, set the coarse control on the computers' DELAY knob to position 2, and press XOE STOP and AUTO RESTART.

6. You should now be able to obtain a trace on the 561 scope showing the output voltages from the X ladder resulting from stepping the B register repeatedly through the numbers 1-2-3.* By adjusting the DELAY knob, it should be possible to produce a picture showing a complete cycle as follows:

* Connecting the ACCUMULATOR ladder output (V13F) to the scope (-) input provides a DC bias which eliminates the need for AC coupling of the signal.



During the flat part of the steps the computer is actually stopped at the three references to register 2 within the program due to the XOE STOP. The machine runs only at the times where the transitions take place. Adjust Potentiometer B_1 (See Fig. 1) so that the heights of the 2 steps are just equal. Use the same asynchronous technique described in step 7 of the X Ladder Adjustment.*

7. By entering the following numbers into RIGHT SWITCHES adjust in turn the corresponding potentiometers:

Number (Octal) in RIGHT SWITCHES	Potentiometer to Be Adjusted
0001	B_1
0003	B_2
0007	B_3
0017	B_4
0037	B_5
0077	B_6
0177	B_7
0377	B_8

* For purposes of synchronizing, note that the first of the three steps must be the one which shows distortion at its onset.

12. Scope Checkout

The following photograph (Fig. 12.1) shows the front of a completed scope module and indicates the position of the various adjusting screws and controls.

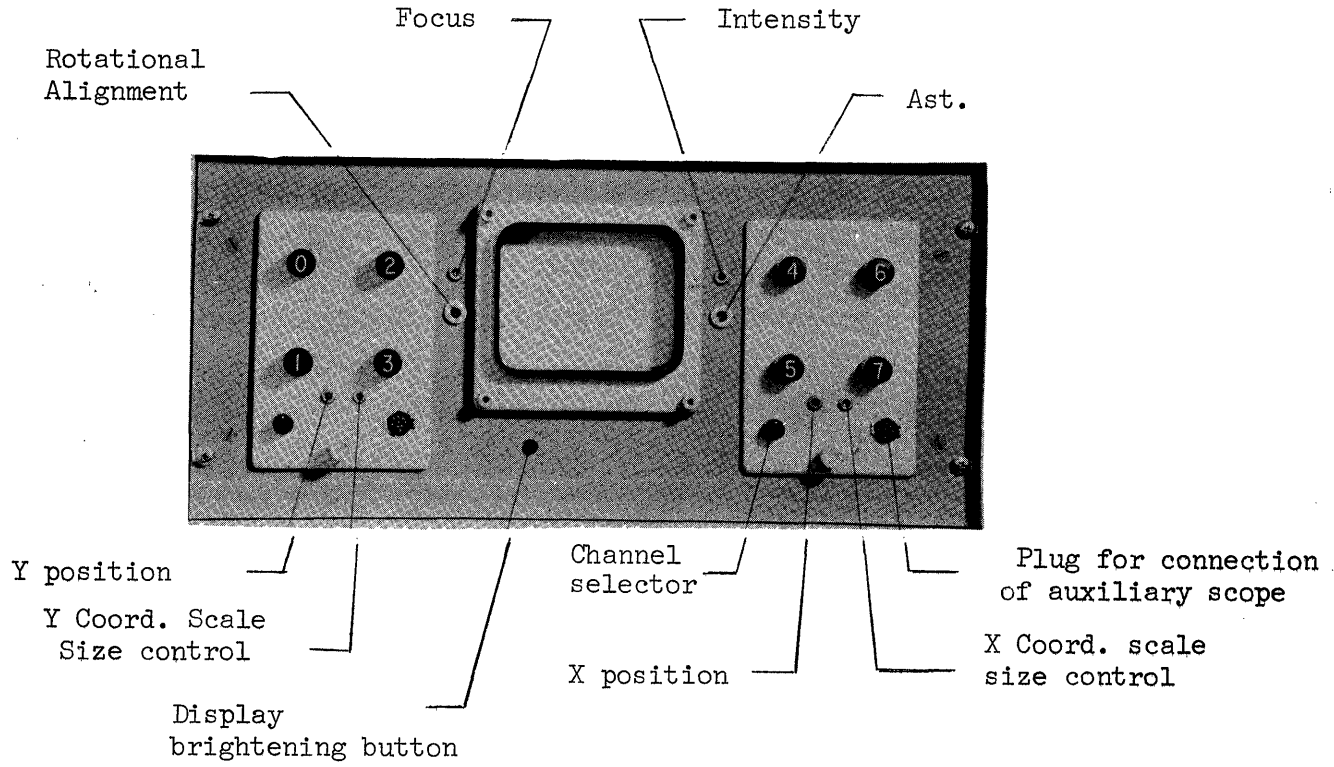


Fig. 12.1

If your scope module has the two special plug-in-units already installed, verify that they have been installed properly according to the ensuing description and photographs. If they have not been installed, proceed to install them as follows:

STEP 1

Select the plug-in-unit with knobs, numbered 4 through 7. This is the right-hand unit. Set the vertical slide switch in the "up" (normal) position and the horizontal slide switch in the Right (i.e., pushed toward the front of the plug-in-unit) position.

(STEP 1, CONTINUED)

Install the right-hand plug-in-unit treating the cable connection as indicated in Fig. 12.2 and Fig. 12.3.

Push the plug-in-unit into place taking care not to damage the connecting cables. Tighten the locking screw down.

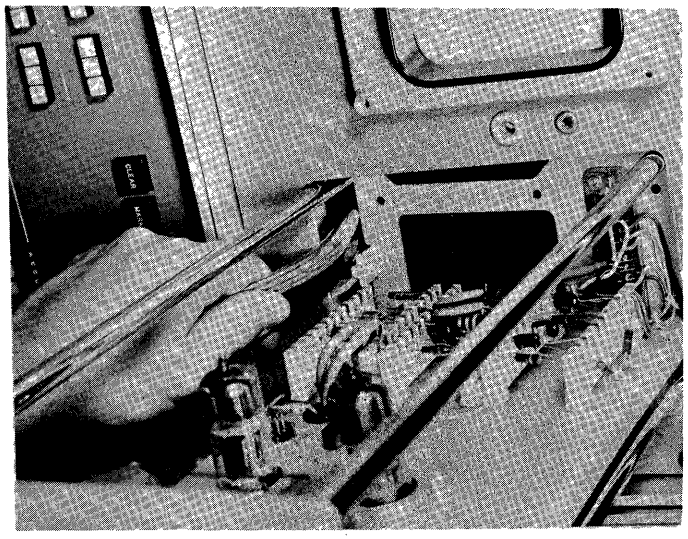


Fig. 12.2

STEP 2

Select the other plug-in-unit and set the vertical slide switch to the "up" (normal) position and the horizontal slide switch in the Left (i.e., pushed toward the rear of the plug-in-unit) position.

Install this unit in the left-hand position in a manner similar to that indicated in Step 1. Note that the left hand unit has only one connecting cable as opposed to the two shown for the right-hand unit.

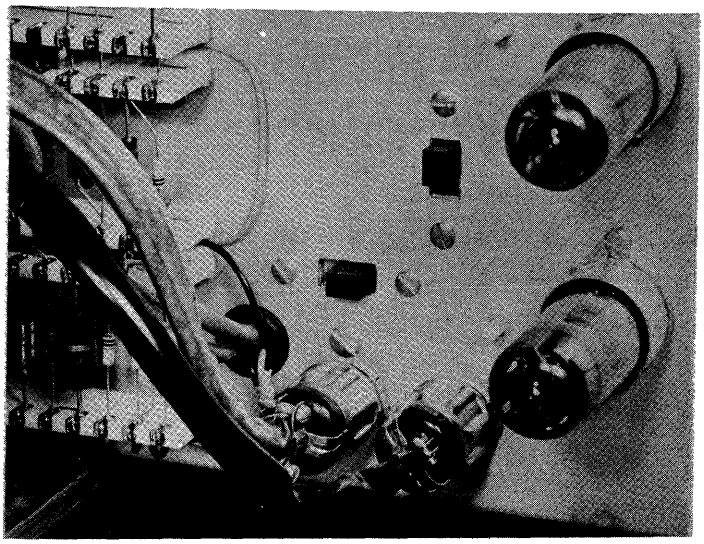


Fig. 12.3

STEP 3

Insert the following program in the memory:

Location	Instruction	Octal
20	CLR	0011
21	DIS i 3	0163
22	JMP 21	6021

Run the program with XOE STOP on location 3 (LEFT SWITCHES) and AUTO RESTART. Adjust delay to observe the counting in register 3 (B lights). Note that the count does not carry out of bit 9, i.e., counting is module 1777_8. Stop the program with the STOP lever and then turn off power.

STEP 4

With power off, install one of the 115 VAC lines from a twist-lock connector at the bottom of the fantail in the main cabinet to the scope unit. Connect the appropriately labled fantail cable from connector FT on the fantail to connector SA on the Scope Module.

STEP 5

WARNING: Overly-bright displays will cause the scope phosphor to burn and can quickly cause deterioration of display quality. Do not, therefore, run any program with persistent displays at a high brightness level. The brightness of a display can be adjusted by the intensity control, indicated in the above photograph. If this control is adjusted properly for one particular display, however, it will not in general be just right for some other display. Specifically, certain displays intensify only a few points and do so at a high repetition rate. This produces a brighter picture than a more complex display that is repeated less frequently. To compensate for these differences the Display Brightening Button is provided. If the intensity control is adjusted properly for a fairly bright picture, then a dimmer picture can be brought up to the same brightness level by holding the Display Brightening Button depressed.

The brightness of the ambient light in the room will effect the apparent brightness of the scope display and thus to achieve maximum clarity with minimum hazzard to the scope phosphor, it is advisable to keep the ambient light level as low as possible.

Turn off power. Verify that the fan at the rear of the scope module is running. Examine memory locations 20, 21, 22 to assure yourself that the program for Step 3 is still intact. Set the channel selection knob on the right-hand plug-in-unit so that the dot is vertical, i.e., so that the switch is in the middle position. (NOTE: the channel selection knob is only effective on the right-hand unit.) Run the program (at full speed) briefly and verify that a horizontal line appears across the middle of the scope. If the line is bright stop the program at once, and turn the intensity control counter clockwise before trying the program again.

Adjust the intensity so that the line is clearly visible but not overly bright. Now momentarily press the Brightening Button and verify that the display brightens accordingly.

STEP 6

Insert the following program into the memory:

Location	Instruction	Octal
20	LDA i	1020
21	-377	7400
22	SET i 3	0063
23	1000	1000
24	DIS 3	0143
25	ADA i	1120
26	1	0001
27	XSK i 3	0223
30	JMP 24	6024
31	JMP 20	6020

Run the program and observe the resultant diagonal line. If the ladder adjustment has been properly and carefully performed, the line will be straight and smooth. If notches or gaps appear in the line, the ladder adjustment should be repeated.

Turn the channel select knob to its fully clockwise position and note that the display disappears. In the other two (middle and counter-clockwise) positions the display will show. Now change the number in location 23 to 5000 and observe that the situation reverses, i.e., the display occurs only with the knob in the middle or clockwise positions.

STEP 7

Insert the following program in the memory:

Location	Instruction	Octal
20	SAM 0	0100
21	ROL 1	0241
22	DIS i 2	0162
23	JMP 20	6020

Run the program. Twist knob 0 and note that you are able to vary the vertical location of the horizontal line. With the knob fully counter-clockwise the line will be at the bottom of the scope. As the knob is turned clockwise, the line will climb to the top of the scope as the knob reaches the fully clockwise position.

Repeat this step for each of the eight knobs in turn, replacing the SAM 0 instruction in location 20 with SAM 1, SAM 2, etc., appropriately as you proceed.

13. Tape Unit Checkout

WARNING: Do not connect the FU-MA cable between the fantail and the Tape Drives until instructed to do so .

STEP 1 - Setting Delays

There are 4 delay units in the cabinet which pertain to tape operation. These delays must be set to proper values before the tape system can operate. The delays, their location in the frame, drawing number references, and proper initial values are as follows:

Name of Delay	Location in Frame	Dwg. No.	Setting
ACIP	T3	1025	120 ms.
TTOK	T2	1023	30 μs.
XTLK	T1	1023	12 μs.
Clock Mark	K12	1023	10 μs.

To set a delay, jumper a PRESET pulse from T7K to pin K of the delay unit. This pulse is produced each time the STOP lever is depressed. Sync the 561 scope on this pulse and with the scope observe the output of the delay unit on pin W. This point will go negative at the time of the pulse and will remain negative for the duration of the delay. The delay may be adjusted with a small screwdriver in the pot accessible through a hole in the rear of the delay unit.*

The ACIP delay will be readjusted to an optimum setting later in the procedure. The other delays remain as set here.

STEP 2 - Resistors and Belt Tension

Verify that the 2 variable resistors mounted on top of the tape electronic chassis at either end are set to their full (100 ohm) value.

Belt tension should be properly adjusted by the manufacturer. This is an important adjustment which enters into operation by affecting acceleration properties and signal stability and strength. Spin the hubs by hand. They should turn freely, and with a sharp flip they should coast for about 5 to 6 turns before coming to a stop.

---

* Before attempting to adjust the ACIP delay, verify visually that pin T3J is grounded and T3H contains no wires. If the reverse is found to be true, correct the wiring by resoldering.

STEP 3 - Checking Write-Current Limiting Parameters

Remove the tape Reader-Writer cards (T20, T21, T23, T24, T25) and inspect them to be sure that on each card, pins P and N are connected only to 100 ohm resistors. These resistors limit current to the tape head (which is an expensive item that can be damaged by large currents).

Replace the cards and turn on power. Insert the following program via the switches:

Loc.	Instruction	Octal Equivalent
40	WGO	0013
41	SAE i	1460
42	0	0000
43	JMP 41	6041

This program causes the writers in all channels to turn over with a 40 μs. period (20μs in one state, then 20μs in the other). Connect a 1K resistor between the ground lead and the tip of a 10X probe. Connect the FU-MA Fantail cable to the fantail but not to the tape unit. Using the 561 scope and the probe with the resistor, inspect the signal at pins 2, 3, 5, 6, 7, 18, 19, 21, 22, 23 of the MA connector on the end of the cable, keeping the ground lead on pin 1. A 25 KC square wave should appear at each of these points between ground and -12 volts. Verify that the amplitude is no greater than 15 volts on any channel. This is the driving voltage for the head write current. If the waveforms are alright, shut off power and connect the cable to the tape unit. Also connect one of the 30' power cords from one of the computer controlled AC outlets at the rear of the power supply to the tape unit.

STEP 4 - Motor Powering Verification

Turn on power. The motors may run on one or both of the units. If this happens press and release the right-hand button on the unit(s). This should bring the motion to a stop.*

On each unit perform the following actions and observe the indicated results:

* A tape unit on which no tape is mounted will frequently run (both motors) when power is turned on or when an MTP instruction selects the other unit. The unnecessary motion can always be stopped by pressing the right hand button on the unit. It can be avoided by keeping tape on both units.

	Action	Result
1.	Press left-hand button	Left motor runs counter-clockwise
2.	Release left-hand button	Left motor continues counter-clockwise Right motor runs clockwise.
3.	Press right-hand button	Left motor stops.
4.	Release right-hand button	Both motors stop.
5.	Do a CHK instruction in togs which selects the unit.	Left motor runs, machine pauses in cycle 2 (0-cycle).
6.	Press Stop lever	Both motors run; pause light goes off.
7.	Press & Release Right-hand button	Both motors stop.

NOTE: The stop lever is the appropriate panic switch for tape operations. It should always stop motion on any unit with a tape mounted and immediately shut off the writers. Always avoid turning power off when tape is moving except in emergencies.

STEP 5 - Reel Mounting

Reels are mounted and demounted from the LINC tape drive by simple snapping on and off from the hubs. A rubber band, hidden beneath the hub's circumferential springs controls the relative ease of mounting and demounting reels.

This rubber band can be adjusted (by replacement) for proper "feel". The reels must be gripped by the hub sufficiently tightly so that no slippage occurs when the motors accelerate (even with some drag on the reel). It should be possible to accomplish this without making mounting and demounting difficult. The reels should have no visible wobble when running.

STEP 6 - Tape Mounting

Empty reels are more or less permanently mounted on the Left-hand hub of each unit. The full reel is mounted on the right hub. The tape is carried across the head to the left reel, stuck to this reel, and wound onto it a turn or two. The left button is momentarily depressed to assume that the tape is adequately mounted. Tape is demounted by winding it off onto the right-hand reel using the right-hand button.

STEP 7 - Head Verification

The following should be performed on each of the two units in turn: Select the unit by 1) entering in switches and MTP instruction which addresses the unit; 2) raising the DO lever; 3) Depressing STOP.

Mount one of the tapes on the unit. Using the 2A63 differential amplifier in the 561 scope, inspect the signal appearing across pins P and N on each of the tape Reader-Writer cards while sweeping the tape backwards and forwards across the head by use of the buttons on the tape unit. A sinusoidal signal of 40 μs. period should be observed in the timing channel. The other channels will show more complex waveforms. The amplitude of the signal in each channel should be at least 5 millivolts (probe to peak). Observe the signal in the timing channel for signs of flutter. This should be inspected at various sweep rates, in order to look for modulating effects at various frequencies. A variation of 10% is normal.

STEP 8 - Noise and Crosstalk

Remove all tapes. Enter a JMP 20 in location 20 and execute the program by pressing START 20. Inspect the noise introduced across the heads (Pins P and N of Reader-Writers) in all 5 channels. Use the 2A63 differential amplifier in the 561 for this purpose, taking care to ground the scope at lower ground lug of T21. The noise should be less than 1/4 mv. in all channels.

Stop the program and jumper the Write Gate input of the timing and mark channels* (pin T21K) to ground. This holds off the timing and mark channel writers. Now enter the following program into memory via the switches:

Location	Contents	Octal Equivalent
40	MSC 13	0013
41	SAE i	1460
42	0	0
43	JMP 41	6041

* These are already connected together.

Press MARK. Look at the signal across pins P and N in the timing and mark channels. This signal is due to crosstalk from the data channels. It should be no more than 15 mv. peak-to-peak in the timing channel and not more than 30 mv. peak-to-peak in the mark channel. After this test, remove the jumper from T21K.

STEP 9 - Instruction Verification

NOTE: Before attempting to perform this portion of the checkout be sure that you are familiar with the operation of each of the instructions. You should understand how the search for a particular block works and how and when re-positioning takes place, so that you know what sort of motions to expect for each instruction. You should also know what to expect in the event of a check sum failure with the instructions RVC, WRC, RCG, and WCG. Do not proceed to later instructions until you completely understand what you observe for earlier ones.

The instructions should now be tested, using one of the tapes included in the kit. Test one unit at a time, by performing on it each of the following instructions in turn from the switches.*

1. CHK - Verify that the CHK instruction is able to locate any block and that after checking, a correct check sum, 7777, is left in the ACCUMULATOR. Verify that successive readings of the same block require one forward (leftward) sweep and one backward (rightward) sweep of the tape. Verify that turning the motion bit on in the instruction causes the tape to be left moving forward (toward the left) following the instruction. Depressing the STOP lever will stop such motion.

2. Do an MTB i (u) 0 and verify that the tape is left moving backward.

3. RDE - this should appear to behave like the CHK instruction. Verify that it does.

4. RDC - If no trouble (error) occurs in reading the block from tape, this will also appear to behave like the CHK instruction.

---

* It will be useful to turn up the audio volume and listen to the S register count as the block is processed. Each time a block is treated you should hear a "chirp" as it is being processed. For RDE, RDC, RCG, WRI and CHK this means a single chirp. For WRC and WCG two successive chirps separated by the repositioning. MTB only locates but doesn't process a block and so no chirp accompanies it.

5. WRI - This instruction is capable of destroying information on the tape, so be careful to specify a block which doesn't contain meaningful information (this can be ascertained from the listing of programs on the tapes). This instruction should make one pass forward over the block and then reposition in front of the block, just as all of the other instructions discussed so far. Clear the memory and do a WRI of quarter 0. Note that the ACCUMULATOR contains all zero's following the write. Now enter a 0001_8 in register 0 and again do a WRI. The ACCUMULATOR is left with 7777_8. Enter a 0002_8 in place of the 0001_8 in register 0 and again do a WRI. The ACCUMULATOR should this time be left with 7776_8.

6. WRC - This instruction, in the absence of any error, makes 2 forward passes across the block, one to write and one to check the information. Verify that the ACCUMULATOR is left with 7777_8.

Before proceeding to test the group instructions (RCG and WCG) perform the following steps:

a) Clear the memory.
b) Fill registers 370-410 and registers 770-1010 with 7777's.
c) Write and check quarter <u>one</u> on some available (unused) block.
d) Clear the memory.
e) Read (RDC) the block back into memory quarter 1.
f) Verify that the following registers have the indicated contents:

Registers	Contents (octal)
370-377	0000
400-410	7777
410-420	0000
760-770	0000
770-777	7777
1000-1010	0000

7. RCG and WCG - Clear the memory and then enter the following via switches:

	Register	Contents
Quarter 0	0	100
	377	377
Quarter 1	400	400
	777	777
Quarter 2	1000	1000
	1377	1377
Quarter 3	1400	1400
	1777	1777
Quarter 4	2000	2000
	2377	2377
Quarter 5	2400	2400
	2777	2777
Quarter 6	3000	3000
	3377	3377
Quarter 7	3400	3400
	3777	3777

Select a set of 10$_8$ available blocks containing no important information. For example, let us assume we have chosen blocks 652 - 661. Using a

WCG
7652

in switches, write the entire memory onto these 10 blocks. The machine should behave as for the WRC instruction although the 2 chirps will be lengthier. The probability of a failure is somewhat higher also inasmuch as more blocks are involved. Verify that the ACCUMULATOR is left with 7777. Now clear the memory, and using

RCG
0652

in switches, read in the first block. In this case it will be block 652 to quarter 2. Verify that locations at the boundaries of this quarter (in this case location 1000 and 1377) have had their original contents restored by the read. Then proceed to

read in the first two blocks of the set with

RCG
1652

in switches. Verify that Quarters 2 and 3 have their old contents.

Now read in all 7 blocks with

RCG
7652

and verify that all quarters have been restored.

The steps performed up to this point assure that the logic of the tape system is in sufficiently good order to proceed to checking other portions of the machine. More comprehensive testing and verification require the use of programs which employ instructions not tested thus far. This more exhaustive testing takes place at a later phase of the assembly procedure. The process of marking other tapes will be tested at that point also.

14. Keyboard Connection

With power off, connect the keyboard cable to the keyboard. Be sure that the sliding bar on the connector locks firmly into place so that the connector does not come unplugged. Plug the other end of the cable into the CH plug at the rear of the console module.

Turn on power and press the small button on the rear of the keyboard near the connector. This should release any key which had been depressed. Note that if you depress a key it will be held down and, furthermore, no other key can be depressed until you press this release button.

Now enter the following program into memory via the switches:

Location	Instruction	Octal Equivalent
20	KBD i	0535
21	JMP 20	6020

Start the program at 20. Note that the computer pauses in cycle 2 (the 0 cycle) of the KBD instruction. Strike the "0" (zero) key on the keyboard. A sharp clicking sound will come from the keyboard as the key is locked down and then released automatically in the process of being read. The ACCUMULATOR should now contain all zero's.

Using the following table, strike each of the keys on the keyboard several times and verify that for each key struck the proper 6 bit code always appears in the right half of the ACCUMULATOR.

Key	6 bit code (octal)
Case	23
0	00
1	01
2	02
3	03
4	04
5	05
6	06
7	07
8	10
9	11
del	13
Q	44
W	52
E	30
R	45
T	47
Y	54
U	50
I	34
O	42
P	43
i	15
A	24
S	46

Key	6 bit code (octal)
D	27
F	31
G	32
H	33
J	35
K	36
L	37
+	20
-	17
#	22
Z	55
X	53
C	26
V	51
B	25
N	41
M	40
p	16
/	21
EOL	12
Space	14

Now place the machine in the INSTRUCTION-BY-INSTRUCTION mode. Note that since the machine is in the paused state, pressing the INSTRUCTION-BY-INSTRUCTION pushbutton will not by itself do this. Instead you must first depress the STOP lever (to get the machine out of the paused state). Then step the machine with the STEP lever until it again pauses. Now strike any key on the keyboard. Note that the machine reads the key and proceeds to the I CYCLE of the JMP instruction. Now press another key. This time the computer is not ready to read the key and thus the key will be held down. Now depress STEP again. This steps the computer to the I CYCLE of the KBD instruction. Still the key is not read. Now depress STEP again. The key code is read into the ACCUMULATOR, the key is released and since a key had been waiting to be read, the computer (instead of pausing in cycle 2 of the KBD instruction) proceeds to the I CYCLE of the JMP, etc.

15. Analog System

STEP 1

Set up the following program in the memory:

Location	Instruction	Octal Equivalent
20	SAM 0	0100
21	JMP 20	6020

Run the program and observe the behavior of the ACCUMULATOR lights as you rotate knob 0 through its full range. With the knob in the fully counter-clockwise position, the ACCUMULATOR should contain -177_8 (i.e., 7600_8). As the knob is rotated gradually clockwise, at first there will be no change. Then the number in the ACCUMULATOR will increase positively as the knob is rotated further until just prior to the fully clockwise position it will have reached its most positive value, $+177_8$ (0177_8).

STEP 2

The Analog Preamplifiers must now be adjusted. Install the Fantail cables which connect to the Terminal Frame Unit. Install the two Analog Preamplifier cards on the forward two slots of the Type "B" Terminal Frame Plug-In-Unit. Install the Plug-In-Unit in the Terminal Unit. Now follow the procedures described in Section 16 to complete adjustment of the preamplifiers.

16. Analog Test and Adjustment

A complete adjustment of the LINC analog system requires first that the digital to analog ladders be checked. This procedure is covered in Section 11. The two simple programs used in the ladder adjustment procedure are included on the TEST tape for convenience. The X LADDER program is on block 211 for memory quarter 0 with a start at 20. The Y LADDER program is on block 212 for quarter 0, and also starts at 20.

Once the ladders have been properly adjusted, there are two adjustment procedures for the analog preamplifiers. If the preamps are badly out of adjustment, use the 0 SET program to bring the preamp offset near zero; then use the ANACAL program.

The ANACAL program is used to set the zero level and gain potentiometers in the analog preamplifiers. A description of 0 SET and ANACAL follows.

The 0 SET program is started by reading block 215 of the TEST tape into memory quarter 0, and starting at 20. Knob 0 is used to demonstrate the method of setting the zero level potentiometers. The program starts by displaying a horizontal line which may be moving up or down on the scope face. The movement can be stopped if Knob 0 is turned to the center of its range. The line will stop moving at some arbitrary vertical coordinate, and may be set to the center of the screen by a momentary operation of Sense Switch 1.

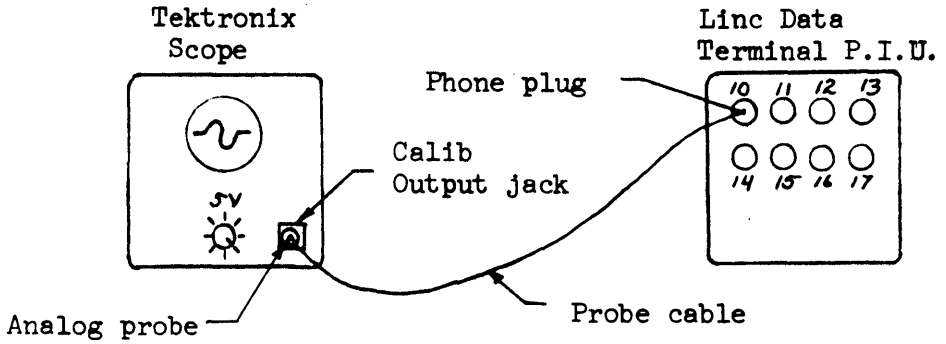


Fig. 16.1

Now strike the 0 key on the LINC keyboard, and the program will sample analog input 10. Adjust the zero level potentiometer for channel 10 until the line stops moving. (See Fig. 16.1) Again, SSW 1 will reset the line to the center of the screen. Do this same procedure for channels 11 through 17 by striking key 1 for 11, 2 for 12 and so forth.

The ANACAL program provides an accurate method of calibrating the analog preamplifiers. The program uses an adaptor probe which is described below.

The Analog Calibrator Probe is designed to provide standard signals to the analog channels of the Data Terminal Box for the purpose of adjusting the analog preamplifiers. These standard signals consist of a positive and a negative square wave, each 0.5 volts in amplitude. A switch is provided on the probe for selecting either positive or negative polarity. The zero volt reference for these two signals is identical.

The probe is attached by the BNC connector to the calibrator output jack on any Tektronix oscilloscope.

The input square wave to the probe from the calibrator should be 5.0 volts in amplitude. This signal can be obtained by setting the calibrator amplitude control to 5.0 volts. The phone plug on the end of the probe cable is inserted into each of the analog channel inputs in turn as successive channels are adjusted. (See Fig. 16.1)

Enter the ANACAL program by reading block 216 of the TEST tape into memory quarter 0 and start at 20. Plug the Adaptor Probe into analog channel 10, and follow the step by step procedure given below for each channel in turn. (For location of the potentiometers and correlation of channels to pots, see Fig. 16.2.)

Channel 14	⌀	Level	⌀	Level	Channel 10
	⌀	Gain	⌀	Gain	
Channel 15	⌀	Level	⌀	Level	Channel 11
	⌀	Gain	⌀	Gain	
Channel 16	⌀	Level	⌀	Level	Channel 12
	⌀	Gain	⌀	Gain	
Channel 17 (not used in Linc P.I.U.)	⌀	Level	⌀	Level	Channel 13
	⌀	Gain	⌀	Gain	

Side View of Data Terminal P.I.U. showing level and gain potentiometer locations on analog preamplifier boards.

Fig. 16.2

1. Connect the phone plug to the desired channel.

2. Set polarity switch on probe to positive.

3. Observe scope presentation for orientation of signal.

4. If lower part of square wave is above the zero level as indicated on scope, the level pot for that channel should be adjusted counter-clockwise until the lower number is ± 000. (See Fig. 17.1) If the lower level is below zero, adjust the level pot clockwise.

5. Once the lower level has been adjusted to zero, read the upper number. If this number is larger than +100, adjust the gain pot for that channel counter-clockwise. If the number is less than +100 adjust the gain pot clockwise. (See Fig. 17.1)

6. After adjustment of the gain pot, the level must be re-adjusted. To do this, repeat step 4.

7. Repeat steps 4 through 6 until the lower number is ± 000 and the upper number is +100.

8. Place the polarity switch on the adapter to neg.

9. Observe the scope for proper signal level. The lower number should be -100. The upper number should be ± 000. Further readjustment of the gain and level pots may be necessary.

10. Final adjustment should yield a scope presentation of a positive transition starting at zero and rising to +100 when polarity switch is pos. and a negative transition starting at zero and falling to -100 when polarity switch is negative.

Repeat steps 1 through 10 for the remaining six channels.

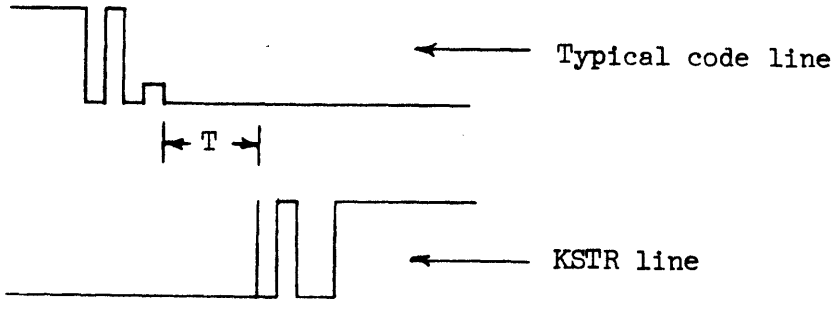
17. Keyboard Testing

Two procedures are given here for keyboard testing. A very simple check of the keyboard codes is performed by Keyboard Test Two. If the keyboard fails during this test, or if the keyboard is known to be failing, use Keyboard Test One. Both of these tests are described below.

KEYBOARD TEST ONE

The most common type of keyboard failure manifests itself as the occasional read-in of an incorrect code. This stems from improper sequencing between the set-up of the 6 code lines and the "common" or KSTR signal which tells the computer that the code lines are ready to be read. It is important that all of the code lines be stabilized (i.e., all contact bounce completed) before the KSTR level goes to ground, signaling readiness.

Each of the 6 code lines is held at ground through a normally closed contact. When a particular key is struck, a specific subset of the six code contacts open, thereby permitting the corresponding code lines to be dropped to -3V by a clamped load. Careful inspection of the code lines will reveal some bounce as the contact breaks. After the appropriate code contacts have opened, and hopefully well after all such bounce is complete, the KSTR level will be brought to ground through a separate set of contacts in the keyboard. This transition will also in general show some bounce. The picture is as follows:

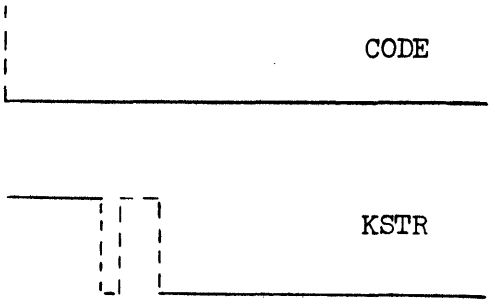


T, for a particular key, is the time between the last bounce on any code line and the first transition of the common line (i.e., KSTR) to ground. T will vary, depending upon which key is struck and sometimes on the way in which the key is struck. The object of testing a keyboard is to determine the minimum T. This represents the safety margin in timing for that keyboard. In general, a keyboard should be adjusted so that this minimum is no less than 1.5 ms. This provides for some decrease which will result from normal wear.

Keyboard Test Program 1

This program requires certain preliminary jumpering to be performed as specified below. This jumpering connects the KSTR level to SAM 10, and each of the code lines in turn to the SAM 11. They are also jumpered to XL_1 and XL_2 for initial transition detection. In order for the program to work properly, the SAM channels must be correctly adjusted.

The program waits for a key to be struck. It then makes certain measurements and presents a display. The typical normal display is as follows:



Margin was 2.13 ms.

This indicates that the time between stabilization of the code line (upper trace) and the KSTR line (lower trace) was 2.13 ms. for this particular striking of this particular key. The code line may sometimes show initial bounce at the beginning of the trace but the time shown will always be the time from stabilization to the first transition of KSTR. Striking any key will prepare the program for the next measurement.

If on any measurement the program detects that the KSTR level makes its transition to ground before the code line makes its negative transition, the comment will so indicate.

If on any measurement the program detects that the KSTR level makes its transition to ground while the code line contacts were bouncing, the comment will so indicate.

Usage:

1) Connect SAM 10 to Frame Pin U24K

   Connect SAM 11 to Frame Pin U24M

   Jumper U24K to U16V

2) Attach one end of a jumper to U24M. The other end will be attached to each of the six code lines in turn. The code line jumper points are given in a table below.

3) Read the program from block 200 of the Test Tape into Quarter 0 and Start 20.

4) To test a key, strike the key. A display will appear on the scope showing activity of the KSTR line and the particular code line to which you are connected. Two cases arise: (See Table following.)

   a) For those keys listed under the code line, the code line should make a negative transition about 1.5 to 3.0 ms. before the KSTR line goes to ground. The display will show the actual time margin. Each key should be tested several times. To repeat the test, strike a key for set-up and then strike the key to be tested again. (The test key itself may be used for set-up.) It may be found that different ways of depressing a key result in different margins or perhaps a failure.

   b) For those keys not listed under the code line, no activity should be noted on the code line. Thus the display will show that KSTR came first. The code line should be inspected carefully for any signs of noise.

Keyboard Test Program 2

This program tests the KBD and KST instructions and the keyboard codes for each key.

Read block 202 of the TEST tape into quarter 1, and START 400.

KB_0 Code Line X17F		KB_1 Code Line X17Y		KB_2 Code Line X14F		KB_3 Code Line X14Y		KB_4 Code Line X11F		KB_5 Code Line X11Y	
Key	Margin	Key	Margin	Key	Margin	Key	Margin	Key	Margin	Key	Margin
CASE		CASE		4		8		CASE		Q	
1		2		5		9		E		W	
3		3		6		del		I		R	
5		6		7		W		A		T	
7		7		Q		E		D		Y	
9		del		R		Y		F		U	
del		W		T		U		G		O	
R		T		Y		I		H		P	
T		O		I		i		J		S	
P		P		i		F		K		Z	
i		S		A		G		L		X	
D		D		S		H		+		V	
F		G		D		J		(#) Tag		N	
H		H		J		K		C		M	
J		K		K		L		B			
L		L		L		-		1-origin			
-		-		-		Z					
Z		(#) Tag		Z		X					
X		X		C		V					
V		C		B		p					
B		p		p		EOL					
N		EOL		SPACE		SPACE					
1-origin											

The program will read in its second block and the words STRIKE ANY KEY will appear on the LINC display scope. When a character key is struck, that character should appear on the display. The space bar and del key will cause SPACE and DELETE to be displayed. The CASE key will stop the display and the LINC will pause. Strike any other key; and if the key has an upper case, that upper case character will be displayed. If the key has no upper case, NOT UPPER CASE will be displayed.

If this program occasionally displays an incorrect character, the keyboard should be tested with Keyboard Test Program 1.

18. Display Scope Adjustment

The adjustment procedure given here uses the SQUARE program for front panel adjustment of the display scope. To start the program, read block 204 of the TEST tape into quarter 1, and START 400.

There are three displays in SQUARE. They are a rectangle, a rectangle with diagonals superimposed, and an array of dots. The rectangles are to be used to adjust the limits of the display area and the array of dots is useful for focus adjustment. Use the rectangle, with or without diagonals for the first round of adjustments. The displays may be indexed forward or backward by striking the F or B keys.

The first display is a rectangle whose sides represent the limits of the display area. That is, the left-hand vertical line represents X = 0, the right-hand vertical line represents X = 777. The top and bottom lines represent +377 and -377, respectively.

Adjust the horizontal and vertical gain and position controls as shown on the picture, to make the display look like a square. Eyeball accuracy is all that is necessary for these adjustments. Now adjust the FOCUS, INTENSITY, ALIGNMENT, and ASTIGMATISM controls to obtain a level, sharp display.

Strike the F key to get the square with superimposed diagonals if this is preferred. Strike the F key again to obtain the focus pattern.

The focus pattern is a low intensity dot array at the center of the display area. Adjust the focus and astigmatism controls for the sharpest dots.

If the B key is struck, the program will return to the previous displays. Any key other than B or F will have no effect.

19. Toggle Switch Testing

There are three toggle switch testing programs. These programs check the SENSE SWITCHES and the RIGHT and LEFT SWITCHES. The programs are described below.

Toggle Test One - SENSE SWITCHES

This is a test of the SENSE SWITCH instruction and the six SENSE SWITCHES. The program indicates a group of bit patterns which are to be manually set by means of the SENSE SWITCHES. Start the program by reading block 206 of the TEST tape into quarter 0 and pressing the START 20 pushbutton.

The computer will halt with the instruction location lights showing 27. The right six bits of the ACCUMULATOR indicate the pattern to be set, where bit zero of the ACCUMULATOR corresponds to SENSE SWITCH 0, bit 1 to SSW 1, etc. A one indicated by an ACCUMULATOR light corresponds to a raised switch. Set this pattern, and raise the RESUME lever. If the pattern actually read in agrees with the given pattern, a new bit pattern will appear in the right half of the ACCUMULATOR. Set the new pattern and again raise the RESUME lever.

If, however, the bit pattern read in is not correct, the LINK BIT will light; and the pattern actually read in will appear in the Left six bits of the ACCUMULATOR. The given pattern will appear in the right six bits, and the program will halt. When such an error occurs, check the switch settings against the right half of the ACCUMULATOR; and raise the RESUME lever again. If the error indication persists, this test will not continue until the problem is corrected; as each time the RESUME lever is raised the same pattern is repeated.

There are 14 (decimal) patterns; and the program repeats endlessly if no non-correctable errors occur.

Toggle Test Two - RIGHT SWITCHES

Toggle Test Three - LEFT SWITCHES

These tests check the LSW and RSW instructions, and the LEFT and RIGHT SWITCHES. Toggle test two is started by reading block 207 from the TEST tape into quarter 0 and pressing the START 20 push-button. Toggle test three is started by reading block 210 of the TEST tape into quarter 0 and pressing the START 20 pushbutton. Except for reading the TEST tape, these two tests have the same operating instructions.

When either program is operating a bit pattern will appear in the ACCUMULATOR, and the program will halt with 27 in the INSTRUCTION LOCATION lights. Set this pattern manually in the RIGHT or LEFT SWITCHES, with bit zero of the ACCUMULATOR corresponding to the right-most switch, bit one to the second switch from the right, etc. Raise the RESUME lever.

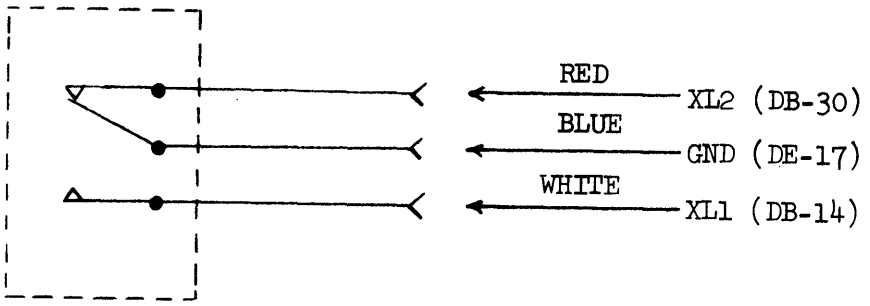
If the pattern actually read in agrees with the given pattern, a new bit pattern will appear in the ACCUMULATOR and the computer will halt. Set the new pattern and again raise the RESUME lever.

If the bit pattern read in is not correct, the LINK BIT will light, and the pattern actually read in will appear in the ACCUMULATOR. The computer will halt at 44. Raise the RESUME lever, and the pattern which caused the error will appear in the ACCUMULATOR. The computer will halt at 27. Check the switch settings against the pattern in the ACCUMULATOR and again raise the RESUME lever. If the error persists, the programs will continue trying the same pattern until the error is corrected. There are 26 (decimal) patterns. The programs repeat the 26 patterns endlessly if no non-correctable errors occur.

20. Relay Testing

The procedure given here tests the LINC relays for operate and release time, and gives a measure of the contact bounce. Due to the nature of the contact bounce, the LINC cannot sample at a rate which would guarantee that all bounces are sensed. During the bounce period, the contacts are closed for 10 to 20 microseconds, and then open for 100 to 200 microseconds; and there may be only two, or as many as a dozen, bounces. The Relay Check program will detect most of the bounces and display them on the LINC display oscilloscope.

The Relay Check program sets all six relays, and then uses an SXL instruction to sense contact closure. Three wires must be connected to the contacts of the relay being tested. These are: a red wire to DB-30 (XL2), a white wire to DB-14 (XL1), and a blue wire to DB-17 (ground). The circuit configuration is diagrammed in Fig. 20.1. It is suggested that the wires be terminated by simple banana plugs to speed up the test procedure. Bring the wires around the side of the plug-in unit so that the banana plugs will reach the relay contact jacks. Plug the three wires into the appropriately colored jacks for one relay, and start the Relay Check program.



The Relay Check program may be put into operation by reading block 213 of the TEST tape into quarter 1, and pressing the START 400 pushbutton. The program will read in its second block and set up the first display.

During operation of the program the line at the top of the display will show contact closure and bounce. The OPERATE and RELEASE times represent the time from the end of an ATR instruction until the first contact closure is sensed. The SETTLED AFTER time represents the time from the end of an ATR instruction until the completion of the last bounce.

Raise SENSE SWITCH 1 to measure OPERATE time repetitively. Lower SSW 1, and the display will show the times for the most recent operation. SENSE SWITCH 2 similarly measures RELEASE time. Watch the contact closure display during repetitive operation for contact bounce.

If a relay should be stuck, the program may sample continuously without finding any contact closure. When this happens push START 400 to restore the program.

21. Display Knobs

The knobs 0 to 7 on the LINC display oscilloscope may be tested with the KNOBS program, which displays the octal value of the knob settings.

To start KNOB, read block 221 of the TEST tape into quarter 0, and START 20.

Manipulate each of the eight knobs while watching the display. Each knob should have a range of +177 to -177.

22. Memory Testing

There are several memory test methods available to the LINC user. The first of these is the memory tuning procedure described in Section 8.

The most frequently used memory test is the CLEAR mode test, which is initiated by pressing the CLEAR button on the LINC console. The CLEAR mode repeatedly checks the entire memory, and leaves the memory cleared when interrupted by any other console function.

Another memory test is the LPFROG program described under Central Logic Tests. The LPFROG program is sensitive to the adjustment of MDEL 2; and the program may be run separately from the Central Logic Test series. See SECTION 2, CENTRAL LOGIC TEST PROGRAMS for instruction about running LPFROG.

Another type of memory test repeatedly reads and writes a special pattern called double checkerboard in the memory. In the double checkerboard pattern, either 0000 or 7777 is stored into a memory location, depending upon its address.

This pattern has the interesting property that reading any of the cores containing ones produces the same polarity voltage across the sense winding. As a result of this property, the double checkerboard pattern produces the largest amplitude spurious voltages when reading zeros and represents a worst case pattern for reading zeros correctly.

The test which is applied to the words which are read back is simply to observe whether the word is all zeros or all ones by means of an AZE instruction. Generally, when a failure occurs it consists of losing one isolated bit or picking up one isolated bit. Thus, any read back memory word which consists of all zeros or all ones will be sensed as zero by an AZE instruction, since both the all zeros and the all ones pattern have the numerical value zero. Although this test is not completely rigorous in that loss or pick-up of all twelve bits in a word will not be detected, such gross failures are unlikely if the memory system is working well enough to operate the test program at all.

In order to test the entire memory, two double checkerboard tests are available on the TEST tape. Memory Test One checks registers 1 through 16 and 103 through 3777 while running in registers 17 through 102. Memory Test Two checks registers 465 through 3777 and 1 through 377 while running in 400 through 464.

Memory Test One is started by reading block 217 of the TEST tape into quarter 0, and starting at 20.

Memory Test Two is started by reading block 220 of the TEST tape into quarter 1, and starting at 400.

When an error is detected, the computer halts with the defective memory word in the ACCUMULATOR, making it possible to determine which bits are failing. The error stop points are register 76 of register 460. If the RESUME switch is raised, the computer will restart and then halt again at register 101 or register 463 with the address of the memory register which failed in the ACCUMULATOR. Resuming once again causes the test pattern to be completely rewritten everywhere and continues the testing.

The program also uses SNS 0 to complement the checkerboard pattern. By alternating SNS 0 from 1 to 0 and restarting, a complemented checkerboard pattern is generated.

Under some conditions, the computer may read the program incorrectly from memory. This may cause a halt in some location other than the ones mentioned above, or some repeated error in executing the program. It is advisable to turn the audio up so that any change resulting from such an error can be detected as a modification of the sound of the program running. The only recourse in this event is to read the program in from tape again and continue, trying the alternate program which runs in the other quarter and tests the quarter in which the program reading failure occurred.

These programs should operate properly with the memory +10 supply varied over a range of +7 to +13 volts.

Double Checkerboard Pattern

Each register of memory contains a pattern which is either all zeros or all ones for each particular register. Whether a register contains all zeros or all ones depends upon its address. All registers whose address bits 1, 5, and 6 contain an odd number of ones (one one or three ones) have the pattern 7777 stored into them. All registers whose address bits 1, 5, and 6 contain an even number of ones (no ones or two ones) have the pattern 0000 stored in them.

Address	Contents	Address	Contents
0000	0000	0075	7777
0001	0000	0076	0000
0002	7777	0077	0000
0003	7777	0100	7777
0004	0000	.	.
0005	0000	.	.
0006	7777	0101	7777
:	:	0102	0000
0035	0000	0103	0000
0036	7777	0104	7777
0037	7777	.	.
0040	7777	.	.
0041	7777	0135	7777
0042	0000	0136	0000
0043	0000	0137	0000
.	.	0140	0000
.	.	0141	0000
		0142	7777
		.	.

23. Magnetic Tape Testing and Adjustment

Testing magnetic tape operation can only partially be performed by programs, even with a tape unit that "works". Complete testing involves looking at signals on the frame with the Tektronix scope. Only after these checks have been made does it make any sense to test the overall functioning of the tape unit with the MTPTST program. The scope investigations are required for two purposes:

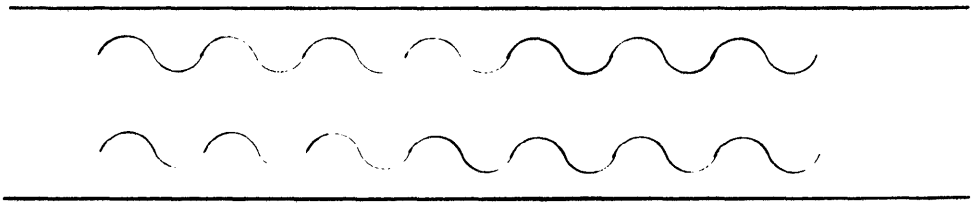
1. To check for proper signal characteristics, and
2. to check the motion behavior.

Signal Characteristics

The primary problems of promoting proper signal strength have to do with getting the tape and the head properly aligned with respect to each other. Inadequate pressure of the tape against the head can also cause a weak or fluttery signal.

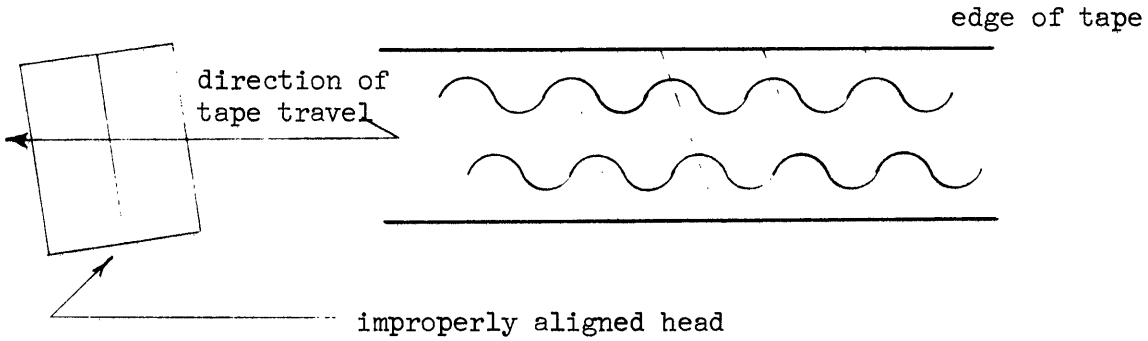
Alignment

The LINC uses redundant recording in two separate tracks on the tape for each of its five logical channels. The two outermost tracks on the tape are combined to form the Timing Channel by adding their sinusoidal signals together. Looking at the tape, the signals may be diagrammatically represented as follows:



In this idealized drawing, the peaks and troughs of the two tracks overlie one another exactly, and adding the two signals together produces a signal of double the individual amplitude. This is the desired goal.

Suppose, however, that the head on which the tape was written was not squarely aligned with the tape. Then the signals on the tape will be offset from one another as follows:



This type of offset is known as skew.

So long as the tape is read on the same misaligned unit, the peaks and troughs will be read simultaneously in the two tracks and thus will add up to give a good signal as before. If, however, we now try to read this tape on a properly aligned unit, the signals will be added together with a phase shift. Instead of the double strength signal, we get a weaker signal characterized by slightly flattened peaks and troughs. The same thing occurs if we try to read a "good" tape on the badly aligned head. Inasmuch as program interchange is dependent upon ability to read tapes made on other machines, it is vitally important that compatibility be retained not only between the two units of a given machine, but between all units of all machines. The timing channel is chosen for discussion and primary checking, because being comprised of the outermost pair of tracks, the effects of skew are most pronounced here.

Heads vary somewhat in their individual sensitivity. In order to make a separate preliminary test of each head's sensitivity, a tape should be marked on a unit and then rerun on the same unit. This eliminates, so far as is practical, alignment variations. A tape marked and read in this way should produce a signal of at least 5 mv. in all 5 channels.* If it does not, the head itself is questionable.

* In order to reverse the units so that the left-hand unit may be used for marking, replace the jumper plug at the rear of the tape chassis with the special jumper plug provided.

The next test is for compatibility with a standard tape. For this purpose the System Test Master tape is to be used. This will present no risk if care is taken not to write on it during testing.

The Master Test tape should be mounted and caused to sweep back and forth by a short program that alternately checks block 0 and 777. Investigation of the signals in the various channels should show approximately the same strength as those derived from a tape marked on the unit undergoing test. A signal of 5 mv. is adequate in any case, whereas a signal below 3 1/2 - 4 mv. can and should be improved by correcting the alignment.

A simple and sensitive test for compatibility involves slight pressure with a finger on the edge of the running tape just to the side of the head. (The pressure should be exerted in a slightly downward direction to avoid raising the tape from the head.) This artificially introduces skew and, if the initial alignment is good, will reduce the amplitude of the signal observed in the timing channel. This should be true for pressure applied on either the right or left side of the head, i.e., for skew introduced in either direction. If this finger test noticeably improves the resultant signal on either side, a skew problem is indicated. In this case the following procedures for correcting alignment should be performed.

Skew Reduction and Mechanical Alignment

1. Remove the Electronic Chassis from the Mechanical Assembly. Exercise extreme caution when disconnecting head cables.

2. Remove the four shoes from the jig plate and keep in pairs.

3. Remove the heads from the jig plate.

4. Remove, if any, all burrs from all clearance holes on the jig plate.

5. Remove all burrs from around the tapped holes in the shoes. (This operation is most important in skew reduction.)

6. Examine the heads. Remove carefully any existing burrs.

7. Shoes should now be polished very lightly by describing a figure 8 pattern using #600 (very fine) sandpaper on a smooth surface. The jig plate functions very well as the smooth surface used in this operation. (Refer to Fig. 23.1)

8. Replace shoes taking care that no foreign material is between shoes and jig plate. For proper shoe alignment refer to Fig. 23.2.

9. Replace heads exercising same precautions as in 8. Refer to Fig. 23.3 for proper head alignment.

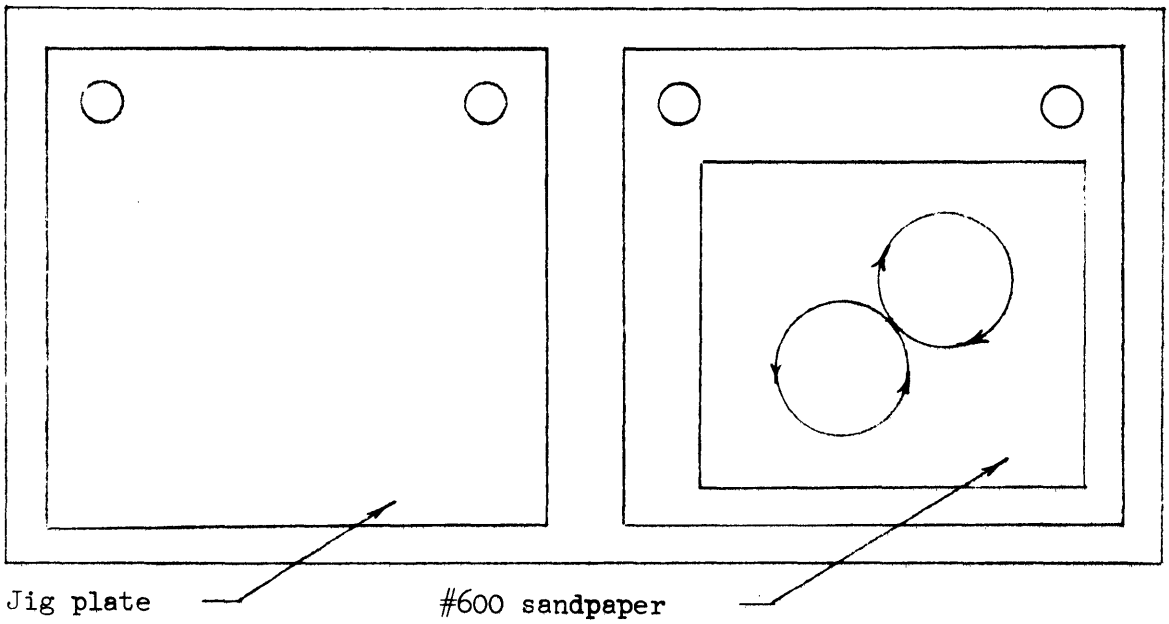


Fig. 23.1

Polish lightly describing a figure 8 pattern as shown above. Approximately 6 cycles. Then rotate shoe 180° and repeat same motion.

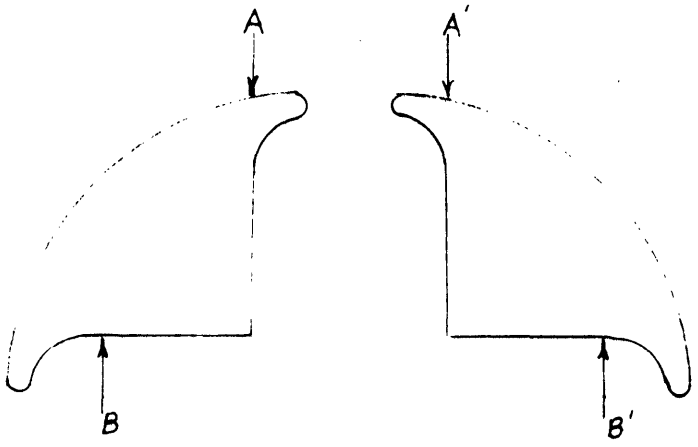


Fig. 23.2

After mounting screws have been partially screwed into shoes, apply pressure in the direction of the arrows at A and B, and then tighten the two screws.

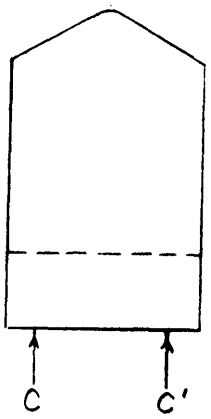


Fig. 23.3

Insert the four mounting screws partially into tapped holes. Apply pressure in the direction of the arrows at C and C', while maintaining perpendicularity of head, and gently tighten screws to a tight fit.

CAUTION: Do not over-tighten screws as this could result in damage to the head.

Weak or Fluttery Signals

If the unit shows a fluttery timing track signal, it may be caused by mechanical jitter of one sort or another resulting in irregular pressure of the tape against the head. Two adjustments are available for improving this situation both of which result in increased drag from the trailing motor. One approach is to tighten the belts on both motors thereby increasing the overall friction and resultant drag. The other approach is to bleed some of the voltage away from the lead motor and apply it to produce opposing torque in the trailing motor. This is accomplished through the variable 100 ohm resistors on the chassis.

Each of these adjustments has an effect on the acceleration properties of the unit; tighter belts tending to result in snappier operation while increased resistor setting makes operation more sluggish. Obviously snappy motion is desirable but as will be seen below, overly tight belts can result in impossible demands being placed on the setting of the ACIP (Acceleration in Progress) delay. Thus a compromise must be reached between these two adjustments which satisfies acceleration requirements while not sacrificing signal stability.

Initial Settings

For a new unit we have found the following rules helpful to get off the ground:

1. Set the variable resistor so that the full 100 ohms is in the circuit.

2. Adjust the belt tension so that the start-up voltage (i.e., the voltage which will just barely keep the hub turning with no tape mounted) is between 15 and 20 volts. This is the best measure of friction resulting from belt tension that we have found. To make this measurement and adjustment, the tape unit is removed from the case and powered through a Variac. The MA cable to the cabinet should be detached. In this condition only the right-hand pushbuttons for each unit will be effective and to make the measurement on the left motors requires switching the motor plugs on top of the chassis.

To make a measurement, run the motor for a bit at full voltage and then gradually reduce the voltage to the point where the motor will just barely continue to turn over.

Crosstalk

Another important test is measurement of the crosstalk which appears in the timing channel while writing in the data channels. Insert the following simple program into the memory via the switches:

Location	Instruction
1	WRI i
2	0
3	LDA i 2
4	JMP 1

This program writes successively in all the blocks of a tape then goes back and repeats the process over and over again. (Be sure to use a tape which you don't mind being completely written over for this test.) Mount the tape on unit 0 and start the program at 1. Now inspect the signal in the timing channel (use the differential pre-amp and direct probes) synchronizing on the signal itself. During the forward sweep down the tape, some crosstalk will appear in the timing channel. (On the backward sweep no writing takes place and hence no crosstalk occurs.) The crosstalk will appear as pulses at the zero crossings of the timing channel signal. Its peak-to-peak value should not exceed 20 mv. If it does, a grounding problem is indicated. If the MTPTST program works without showing errors, it is not serious. If, however, errors occur in MTPTST and crosstalk is high, the grounding must be carefully checked and corrected to reduce the crosstalk amplitude.

Motion Behavior

Both the speed and acceleration characteristics of the units are important.

Speed

The speed of a tape unit may most easily be checked by looking at tt_0 pulses derived when sweeping the System Master Test Tape from end to end under program control. Use a program which alternately checks blocks 0 and 777. The tt_0 pulses should ideally come every 40 μs. while the tape is running at normal speed in either direction. Some variation may be noted from one end of the tape to the other but the inter-pulse interval should lie between 37 and 43 μs.

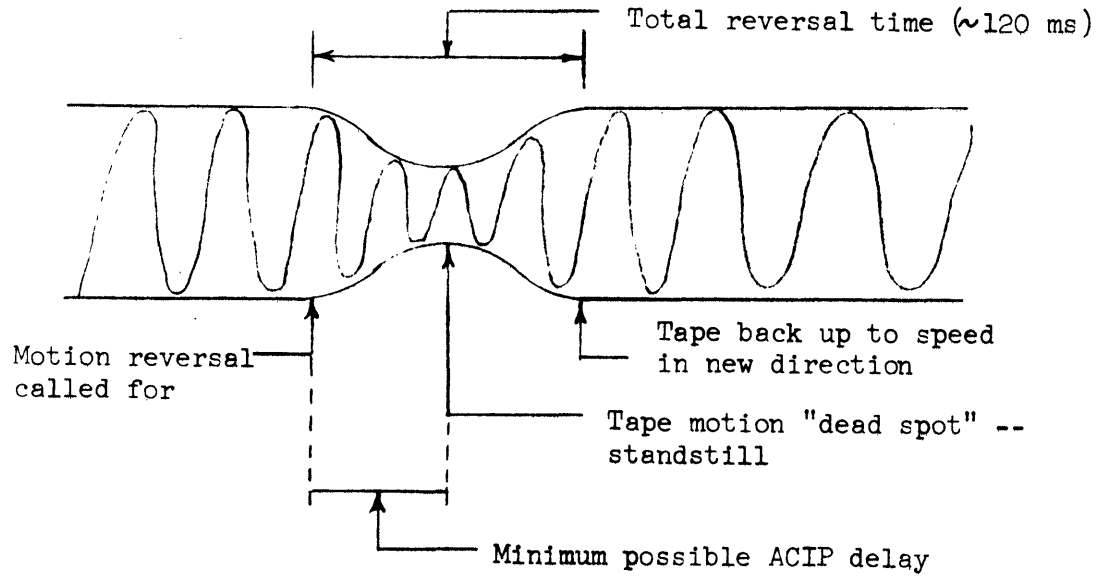
Various factors effect the speed. First of all be sure the tape shoes are clean and dry. High humidity can bring a normal unit to a standstill, so don't attempt to check speed in exceptionally humid conditions. Two factors over which you have control are the tightness of the belts and the amount of voltage deflected to the trailing unit through the variable resistor on the chassis. However, while these factors have a first order effect on the acceleration properties, their effect on speed is secondary. When adjusted for proper acceleration (see below) they should provide proper speed.

Acceleration

The criteria for proper acceleration characteristics stem from various, sometimes conflicting, demands on the Acceleration In Progress (ACIP) delay. In the acceleration tests it is not necessary to use the test tape. Any reasonable marked tape will do.

ACIP Lower Bound -- This delay must be at least long enough so that whenever a change in direction of motion occurs the delay runs until the tape has gained enough speed in the new direction to produce reliable signals in the timing channel. This requirement must hold for forward-to-backward and backward-to-forward changes on both units and at all positions on a tape. The worst case of this sort places the lower bound on the setting of ACIP.

When a reversal of direction occurs it is manifested by a momentary drop in the amplitude of signals from the tape as follows:



(An even sharper "bite" in the signal sometimes is visible immediately following the call for reversal. This is apparently due to momentary lifting of the tape from the head as the motor voltages are reversed. It is of no consequence here.)

This reversal may best be observed by looking with the differential amplifier at the timing track signal.* The scope sweep should be synchronized on transitions of the $MOTN_0$ flip-flop. A program which repeatedly checks a block should be used. By synchronizing on the transition of $MOTN_0$ to a "1" the scope will sweep each time the reversal from forward to backward occurs. A careful measurement should be made of the time from the beginning of the sweep until the "dead-spot" in the motion occurs. The sweep should now be synchronized on the opposite transition of $MOTN_0$ (to a "0") and a similar measurement made for the time between the reversal to forward and the ensuing "dead-spot". These two measurements must be made at both ends of the tape (block 0 and 777) and on both units. The readings should be recorded on a chart similar to the one shown in Fig. 22.4. The longest of all of these readings places the lower bound on the possible settings of ACIP.

ACIP Upper Bound -- The upper bound on ACIP is set by one of two requirements:

1. In searching backward down the tape for a particular block, the delay must not be set so long that after the decision to reverse and go forward is made the delay is still running when the desired block is encountered going forward.

2. Following a turn-around and stop maneuver at the end of a tape instruction, the tape is brought to a standstill somewhere in front of the referenced block. The delay must be short enough so that in starting forward from this position it will have timed out before the block is again encountered.

Before attempting to make these measurements, the ACIP delay should be set to the figure just determined as the lower bound. Now run the program which repeatedly checks a block and synchronize the scope on the reversal to forward (i.e., the transition of $MOTN_0$ to "0"). Finding of the requested block is indicated when the CHK instruction enters cycle 3. Measure the time from the call for forward to the rise of CY3. (If the unit rocks back and forth never entering cycle 3, difficulty with the left-hand motor is indicated. Interchange of the left and right motors on the unit may help in this case.) Record this value in the table for blocks 0 and 777 for both units.

---

* For this purpose direct probes will be required for adequate precision of readings.

UNIT 0

BLOCK 0 FWD -- BWD	
BWD -- FWD	
BLOCK 777 FWD -- BWD	
BWD -- FWD	

LOWER BOUND = [ ] = Largest of above figures

FWD -- CY3 BLOCK 0	
BLOCK 777	
RESUME CY3 BLOCK 0	
BLOCK 777	

UPPER BOUND = [ ] = Smallest of above figures

Proper Setting = $\frac{\text{LOWER BOUND + UPPER BOUND}}{2}$ = [ ]

Margin = UPPER BOUND - LOWER
Should be at least 20% of proper setting.

Now, using I STOP, stop the machine on the CHK instruction.* Change the synchronization of the scope so that it sweeps on the transition of $MOTN_1$ to a "1". Leaving I STOP set, each time the RESUME lever is raised the requested block should be checked and the tape repositioned in front of the block. Allow the tape motion to come to a stop each time before RESUMING. On each RESUME, the tape should make one sweep forward and then one backward and come to a stop.

If other reversals occur they indicate that the tape is not repositioning sufficiently far in front of the block. This may be verified by a slight additional manual rewind following the stop each time. The only solution to this difficulty is to loosen the belts, but before resorting to this major operation, be sure that there are no other mechanical binds. In particular be sure that the shoes are clean. Dirty or moist shoes can drastically cut the coast-to-stop distances. If belt loosening is required the acceleration tests must be begun over again after the unit is reassembled.

In loosening the belts, it will probably be necessary to reset the variable resistors to a higher value in order to maintain a good stable signal from the tape. Looser belts cause reduced drag with resultant loss in tape tension against the head. This must be compensated by increased voltage being shunted to the trailing motor. This is accomplished by increasing the value of the variable resistors. In most cases we have found it advisable to set the resistors to their full (100) value. This, combined with loosened belts, results in slightly more sluggish operation but in greatly increased reliability.

Taking now the happier alternative, if the motion seems proper, measure the time from the start of sweep to the onset of cycle 3. Once again record this measurement for block 0 and 777 on each unit.

The shortest of the last 8 measurements places the upper bound on the setting of the ACIP delay.

The proper setting of the ACIP delay for this pair of units is the average of the upper and lower bounds. The amount of margin is indicated by the difference between the two and should be at least 15% of the average. If it is greater than 40% of the average, the motion can be made snappier by reducing the value of the variable resistor somewhat. This will in general reduce signal stability which will require tighter belts to compensate. A new set of measurements must then be made to determine the new limits on the setting of ACIP.

* Be sure that the motion bit is not set on the CHK instruction.

MTPTST: Magnetic Tape Test Program

The program runs a reasonably exhaustive test on the selected tape unit. A good marked tape, which should contain no useful information, is written and read at every block with a complex pattern. The test requires several minutes to run.

The magnetic tape test program is entered by reading block number 205 of the TEST tape into quarter 0, and starting at 20.

The program will rewind unit 0 and halt. Mount a marked tape which contains no useful information on either unit 0 or unit 1. SENSE SWITCH 1 controls the unit to be tested. SSW 1 down is unit 0, and SSW 1 up is unit 1. After mounting the tape and setting SENSE SWITCH 1, raise the RESUME lever, and the test will proceed.

A pattern is generated in Q_1. This pattern is written in block 777 with a WRI instruction. The block is then read into (previously cleared) Q_2. Q_1 and Q_2 are compared bit for bit. If no errors are found, the pattern is written in successively lower block numbers, the test stops at block 0 with a halt at Location 140. After every other read (i.e., for every other block) a programmed delay occurs to permit repositioning. Ordinarily repositioning will carry the tape far enough back so that on restarting, a block one block in advance of the previously referenced block can be picked up from standstill.

Thus, typical motion during the test should be:

Forward to read block i-1

Coast back and pause

Forward to write block i

Backward

Forward to read block i

Backward

Forward to write block i-1

Backward

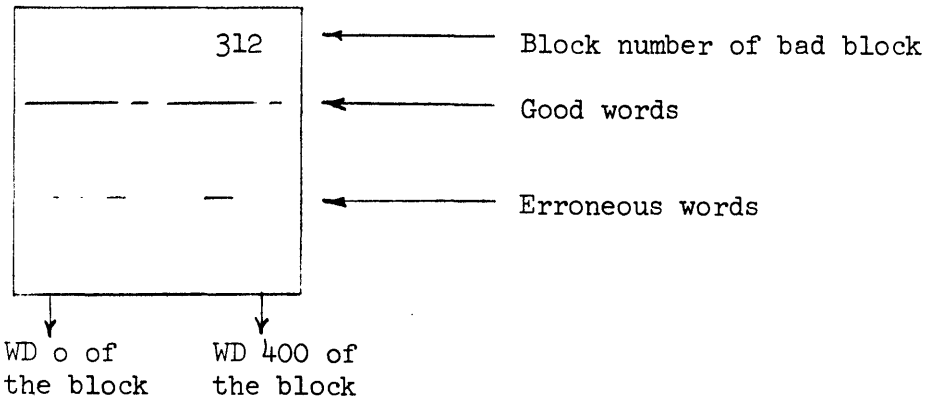
This places an additional demand of one extra block on the repositioning distance. If more reversals than those listed occur between pauses, trouble is not necessarily indicated. However, it means that you should

test the repositioning by checking block 0 with a

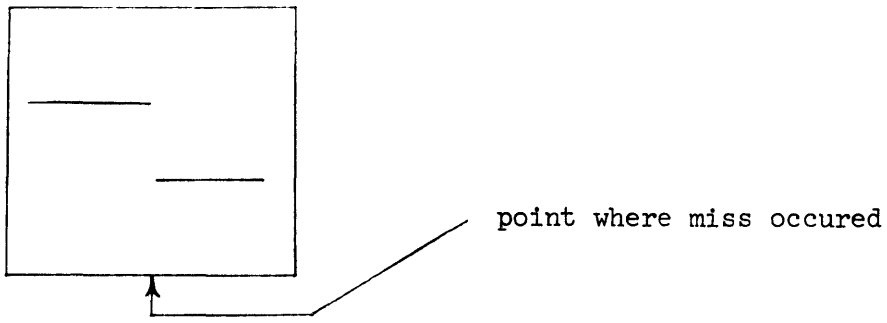
CHK	0707
0	0000

in switches. On successive raisings of the DO lever, the tape should make just one pass forward over the block and then should reposition. If more reversals are required, the tape unit is in need of adjustment. Block 777 should be checked in the same way.

If an error occurs on any block a display will appear showing the erroneous words of the block as follows:



If a word is missed in either writing or reading the block, all of the words from that point on will be read into the incorrect location in memory and a display of the errors will be as follows:



If this sort of trouble occurs on more than one or two blocks on a tape it suggests crosstalk problems. Momentarily, raise SSO to continue testing after an error display.

24. Marking Tapes

Using tape head cleaner (Carbona), clean both sets of heads and shoes thoroughly. Mount the TEST tape on unit 0, and with a toggle instruction, read block 223 into quarter 0 of the memory. START 20 to remove the tape from unit 0, and mount a degaussed tape on unit 1, pulling just one full turn of tape onto the lead reel. After the tape on unit 0 has been removed, press the MARK button.

The program will start the right-hand tape running continuously, and will mark the tape. When the program halts at location 217, rewind the tape partially by hand by holding the right-hand button depressed for 10 seconds or more. Then raise the RESUME lever.

The program will proceed to check the tape for proper marking. A final stop at location 310 indicates a good tape. A stop at 305 indicates an improperly marked tape, in which case the mark process should be repeated. First degauss the tape, and verify that the head and shoes are still clean.

To remark a tape, or to mark another, the MARK program need not be read in a second time. Pressing the MARK button will cause it to start marking the next tape.

Precautions

For best results:

1. Check the mark clock. It should be set to 10 μsec.
2. If the tape is new, manually run it across the head a few times to align it on the reels and remove loose oxide.
3. Make sure head and guides are clean after the above operation.

25. Finale

Accept our warm congratulations! You now have a working LINC.

LINC Volume 15

Assembly and Test Procedures

Section 2

CENTRAL LOGIC TEST PROGRAMS

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CENTRAL LOGIC TEST PROGRAMS

Contents

CENTRAL LOGIC TEST PROGRAMS

1. Introduction

These programs consist of functional tests of the LINC instructions, and tests of some of the logical areas of the machine. Functional tests are written without regard to the detailed logic of the computer, but are based entirely on the written functional description of the instructions. As such, they represent a confidence check of the LINC. They offer no real diagonostic information, but only indicate that a failure has occurred. Their main value is in the detection of errors and the fact that if they run successfully, the machine is probably sound.

2. Control Program Operating Instructions and Common Information

A. Central Program

Since the test programs are capable of automatic execution, they are preceded by a control program (CONTRL) in block 0 of the tape. The control program resides more or less permanently in quarter 0 of memory. The coding in 20-22 reads in the next block from tape into quarter 1 and then jumps to 401 to execute the program. It is initially set up to read block 1 into quarter 1. This then is the normal entrance to start executing the programs. Location 21 may be examined to find the block number last read in. This may then be looked up in the index to find the program currently being executed.

In addition to the entrance at #1R (20), there are some other entrances to the control program. The entrance at #1A (23) is used to read block 1 after the control program has been used and the contents of 21 have been changed. The entrance #1T (34) is used to read the next test. This is where each of the separate programs returns after execution of the program. The entrance at #1B (41) is used to read a specific block. The block number is contained in the LEFT SWITCHES. It may seem that it would be simpler to read a specific block by performing a read operation from the switches. This is all right if only that one block is required. But if it is desired to continue operating additional programs or because some programs are more than 1 block long, it is best to use the #1B (41) entrance to (CONTRL).

Location #1I (46) contains an increment to the block counter. Since programs that are more than one block long are responsible for reading themselves in, the variable increment is necessary to insure that a return to #1T (34) reads in the next test and not just the next block. Location #1V (47) contains a constant which identifies the collection of programs. It is currently 1002.

B. Operating Instructions

The normal use of the control block is to do 0700 0000 from the switches and then do a START 20. The machine should immediately halt with 401 in the INSTRUCTION LOCATION lights. Put 300 in the RIGHT SWITCHES, 700 in the LEFT SWITCHES, and 77 in the SENSE SWITCHES. Turn KNOB 0 fully clockwise.

Now raise the RESUME lever and each of the test programs will be read in and executed.

As mentioned before, a start at 41 will cause the test series to be started at a program selected by a block number in the LEFT SWITCHES. After such a start, the pattern 0700 0300 must be restored to the switches before the program MISCTS runs.

There is the possibility that the Marginal Check Voltages may be changed while running the programs. However, the real danger exists of destroying the tape. It is recommended that a specific program be read in, modified in memory to continuously run, and then the tape removed before doing any marginal checking.

C. Common Features of Programs

All of the programs are written to be initially read into quarter 1 and started at 401. If the program needs more blocks or if it must run in another quarter, it makes these modifications. The test number is stored in location 400 if it is at all possible. Sometimes this is not possible and then the test number is stored in the first location of a quarter. Some programs modify quarter 0 in the course of their execution. These programs take care to save the control program and then restore it to quarter 0 when they are finished. The one exception to all of this is the Leapfrog (LPFROG) program. It continuously runs and moves through all of memory. Therefore, it is stored in the last active block of the tape.

The comments on the test programs refer to patterns called FLOAT 1 and FLOAT 0. These are numbers which have only one bit set or one bit cleared in a string of the opposite bit values.

FLOAT 0	FLOAT 1
7776	0001
7775	0002
'	'
'	'
5777	2000
3777	4000

In each test program the essential instructions are marked by a bracket to the left in the manuscript. For example, Test #2, BCLTST contains the following sequence:

```
0412        LDA i
0413        7777
0414        BCL i
0415        7777
0416        SAE i
0417        0
0420        HLT
            '
            '
            '
```

Should the above sequence of instructions detect an error, you might want to execute continuously that portion of the test. To do this the SAE i in 0416 could be changed to a JMP 0412. Starting at 0412 would then effect a continuously running loop in order that waveforms could be examined on an oscilloscope. This change should only be made to the program in memory and not made permanent by writing the block on tape.

In the following sequence of instructions from the same programs, indexing is used within the bracketed instructions. Therefore, the BCL i 3 in 477 should be changed to a BCL 3 before reentering the loop.

```
0445        #2B  LDA i
0446             7777
0447             BCL i 3
0450             SAE i 4
0451             HLT
                  '
                  '
```

Another useful modification to a program in memory is to change the instruction JMP 1T, which returns to the control program, to a JMP 2A instruction which will allow the program to be continuously cycled without reading any new programs. This is useful when varying the Marginal Check Voltages.

This collection of test programs should not be considered to be a big program with many separate parts. Rather, it should be viewed as small, self-contained programs put on tape with a simple control program to execute them one at a time. If at anytime you are interested in only one of the programs, do not hesitate to read it in by itself and then run it.

3. Test Programs

On the following pages are brief descriptions of each of the individual test programs. Following the program descriptions are copies of the manuscripts, including comments, of all of the programs on the Test Tape. The descriptions and manuscripts are in the order in which the tests appear on the Test Tape. This is not exactly the same as increasing numerical order of the test numbers.

TEST #70 HLTTST

The first instruction test program must exercise the HLT instruction since all the following tests use the HLT instruction to indicate errors. The machine will halt with 401 in the INSTRUCTION LOCATION lights, and the test series may be continued by raising the RESUME lever.

TEST #1 SAETST

This is the basic test of the SAE instruction. The first four sub-tests check all four combinations of 7777 or 0000 in the ACCUMULATOR and the number specified by the SAE instruction. The last four sub-tests loop through the same combinations but with FLOAT 1 and FLOAT 0 patterns.

TEST #2 BCLTST

TEST #3 BSETST

TEST #4 BCOTST

These are the basic tests of the three bit-manipulation instructions. BCL, BSE, and BCO. Each of the three tests is organized in the same way. The first four sub-tests check the four combinations of 7777 or 0000 in the ACCUMULATOR and the number specified by the test instruction. The last four tests continue with 7777 or 0000 in the ACCUMULATOR, but the number specified by the test instruction is a member of the FLOAT 0 or FLOAT 1 patterns.

TEST #5 ROLT1

TEST #6 ROLT2

TEST #7 ROLT3

TEST #10 ROLT4

TEST #11 ROLT5

These are the basic tests of the ROL instruction. Tests 5-10 are similar and loop through all combinations of rotate counts, i.e. 0-17, with all eight combinations of FLOAT 0 or FLOAT 1 patterns and i-bit equal to one or zero. The conditions are specified by comment lines at the beginning of each program. Test #11 is similar except that the patterns are 7777 or 0000 instead of FLOAT 0 or FLOAT 1.

TEST #12 RORT1

TEST #13 RORT2

TEST #14 RORT3

TEST #15 RORT4

TEST #16 RORT5

These are the basic tests of the ROR instruction. Tests 12-15 are similar and loop through all combinations of rotate counts, i.e. 0-17, with all eight combinations of FLOAT 0 or FLOAT 1 patterns and i-bit equal to one or zero. The conditions are specified by comment lines at the beginning of each program. Test #16 is similar except that the patterns are 7777 or 0000 instead of FLOAT 0 or FLOAT 1.

TEST #17 CLRTST

This is a test of the CLR instruction. It is extremely simple. It loads the ACCUMULATOR and the LINK BIT with ones and then checks that the CLR instruction clears both the ACCUMULATOR and the LINK BIT.

TEST #20 ADDONE

This test is a little tricky. It checks the operation of adding one to the ACCUMULATOR against the indexing by one in the B register. The trickiness results from the operations necessary to insure that bits 11 and 10 are properly set in the index register. Since the operations are checked against each other, there is no absolute answer provided; that is, the trouble could be in the ACCUMULATOR or in the indexing of the B register.

TEST #21 COMT1

This is a test of the COM instruction. Both the test constants and test results are completely specified by the two tables, #2T and #3T. The program is extremely simple and needs no further comment.

TEST #22 SCRT1

TEST #23 SCRT2

TEST #24 SCRT3

TEST #25 SCRT4

These are the basic tests of the SCR instruction. They are similar and loop through all combinations of scale counts, i.e. 0-17, with all eight combinations of FLOAT 0 or FLOAT 1 patterns and i-bit equal to one or zero. The conditions are specified by comment lines at the beginning of each program. The SCR instruction does not form a ring as in the rotate instructions, so there is no simple way of computing the test result. Therefore, all of the results are completely described by constants read in from the tape. This results in a rather large number of constants, especially in the case where i=1. In fact, when i=1 the tests require two quarter of memory. This does result, however, in a rather straightforward test of a somewhat complex instruction.

TEST #26 ADDT1

This is a test of the ADD instruction. It is extremely simple and the only loop is to control the number of times the complete test is done.

TEST #27 FADRT1

TEST #30 FADRT2

These are tests of the full address instructions, ADD, STC, and JMP. Each test loops through two quarters of memory, storing a JMP 0 at only one memory location. Then a JMP to this location is executed and the program should return, through 0, to the main program. Since most of the memory is cleared, a JMP to the wrong place should halt the computer. Test #27 places JMP 0 in quarters 2 and 3 and Test #30 places them in quarters 0 and 1. Since Test #30 destroys the control program in quarter 0, it saves quarter 0 in quarter 3 and then restores it when finished. The main body of the program is in quarter 2, so look for the test number in location 1000 as well as 400.

TEST #31 iBETA1

This is a test of the index class of instructions with i = 0 and β = 0. The test stores a unique constant at every location in Q2 - Q7. The constant is the address plus 2^{11}. Then the contents at each location are loaded by an LDA X and checked against the constant stored at a location in Q1.

TEST #32 iBETA2

This is a test of the index class of instructions with i = 1 and β = 0. The test stores a unique constant at every location in Q2 - Q7. The constant is the address plus 2^{11}. Then each address is loaded by an LDA i X instruction and checked to insure that the 2^{11} bit is not present. In other words, the address itself should be loaded into the ACCUMULATOR.

TEST #33 iBETA3

This is a test of i-β addressing when i = 0 and β = 1 - 17. The test stores a unique constant at every location in Q2 - Q7. The constant is the address plus 2^{11}. Then the address is stored in a β register. The contents at each location are loaded by an LDA β instruction and checked to insure that the proper constant has been loaded.

TEST #34 iBETA4

This is a test of i-β addressing when i = 1 and β = 1 - 17. The test stores a unique constant at every location in Q2 - Q7. The constant is the address plus 2^{11}. Then the address -1 is stored in a β register. The contents at each location are loaded by an LDA i β instruction and checked to insure that the proper constant has been loaded. Some extra programming is required to get around the discontinuity in addresses in going from Q3 to Q4. The trouble occurs when the β register should be indexed from 1777 to 2000. To get around the problem and still test for proper indexing, 3777 is stored in the β register and then the incrementing gives 2000.

TEST #35 LDAT1

This is a test of the LDA instruction without regard to i-β addressing. The numbers 7777 - 0000 are loaded into the ACCUMULATOR and then the numbers 0000-7777 are loaded by an LDA. The contents of the ACCUMULATOR are checked and then the contents of the operand location specified by the LDA are checked.

TEST #36 STAT1

This is a test of the STA instruction. All possible combinations of 12 bits are stored in memory from the ACCUMULATOR. Then the contents of the ACC and the contents of the memory location are checked.

TEST #37 ADMT1

This is a test of the ADM instruction. The ACCUMULATOR and C(Y) are counted up from 0 to 7777 and then compared to a count which has been generated by increasing a β register in the B register. This tactic is the same as that used in Test #20, ADDONE.

TEST #40 LAMT1

This is a test of the LAM instruction. It uses 11 sets of values for initially loading the ACCUMULATOR, the LINK BIT, and the contents of the memory location referenced by the LAM. Then the LAM is executed and the results in the ACCUMULATOR, contents of memory, and the LINK BIT are checked. The program is straightforward with all of the test values read in with the program as constants.

TEST #41 MULT1

This is a test of the MUL instruction. The general scheme is to multiply the pairs:

(0000) x (0000)
(0000) x (1111)
.
.
.
(0000) x (7777)
(1111) x (0000)
(1111) x (1111)
.
.
.
(1111) x (7777)
.
.
.
(7777) x (7777)

by both integer and fraction multiply. The results are then checked against those read in with the program as constants. Then the LINK BIT is checked to insure that it is equal to the sign bit of the result.

TEST #42 SROT1

This is a test of the SRO instruction. All possible combinations of a 12 bit number are checked. The results are generated by a ROR 1 instruction. Then the decision is made as to whether or not the number will generate a skip. The check for the skipping operation is then made up accordingly.

TEST #43 SETT1

This is a test of the SET instruction with i = 0. The test stores all combinations of 12 bits in all β registers (0 - 17).

TEST #44 SETT2

This is a test of the SET instruction with i = 1. The test stores all combinations of 12 bits in all β registers (0 - 17).

TEST #45 XSKT1

This is a test of the XSK instruction with i = 0. It loads all combinations of 12 bits into β registers 1 - 17. For each value, the program checks to see if a skip will occur on the XSK instruction and modifies the checking part of the test accordingly.

TEST #46 XSKT2

This is a test of the XSK instruction with i = 1. It is similar to XSKT1 (Test #46), with the added complexity of computing the value

of C(β) after the indexing. Special care is needed because of the manner of the index add operation.

TEST #47 AZET1

This is a test of the AZE instruction. The numbers +0 and -0 are checked to see that skipping does take place. Then non-zero patterns, consisting of floating 1 and floating 0 are checked to see that skipping does not occur. The patterns are all included as constants in the program.

TEST #50 APOT1

This is a test of the APO instruction. Patterns consisting of floating 1, floating 0, +0, and -0 are checked. The patterns are all specified as constants in the program.

TEST #51 LZET1

This is a test of the LZE instruction. The patterns floating 1, floating 0, +0, and -0 are checked in the ACCUMULATOR with C(L) = 1 and C(L) = 0. All patterns are specified as constants in the program.

TEST #52 HWCT1 i = 0, Beta = 0

This half-word class test uses LDH and STH to store bit patterns into the left and right halves of memory locations from 1000 to 3777. Both halves of the stores pattern are compared to the given pattern, and the program halts if a mis-match appears.

TEST #53 HWCT2 i = 1, Beta = 0

This half-word class test loads bit patterns into memory locations from 1000 to 3777. The LDH i and STH i instructions store and retrieve

the patterns. The left half of the stored pattern must agree with the given pattern.

TEST #54 HWCT3 i = 0, BETA = 1 - 17

This is a test of the half-word class instructions with i = 0 and BETA $\neq$ 0. The STH B instruction is used to store the right half of the ACCUMULATOR in first the left, then the right half of memory locations 1000 to 3777. Each memory address is loaded with a unique number which is the address plus 4000. The program steps through all 17 BETA registers.

TEST #55 HWCT4 i = 1, BETA = 1 - 17

The test is similar to HWCT3, except in the manner of incrementing the BETA registers.

TEST #56 HWCT5

This is a test of the SHD instruction. All combinations of SHD β are tested. The comments beside the error halts in the manuscript give the bit patterns which were compared by the SHD instruction.

TEST #57 RANADD

This test performs additions with numbers generated by a pseudo-random number generator. The sequence of operations is clearly indicated on the manuscript.

TEST #60 ATRT1

This test checks the logic paths from the ACCUMULATOR to the RELAY REGISTER.

The program interchanges patterns of bits between the ACCUMULATOR and RELAY REGISTER. If an error occurs, the computer will halt at location 432 with the LINK BIT lit. The bit pattern which caused the error will appear in the right six bits of the ACCUMULATOR, and the bit pattern actually transferred will appear in the left six bits of the ACCUMULATOR.

Raising the RESUME lever will cause the program to try the offending pattern again.

TEST #61 IBZT1

This program checks the functioning of the IBZ instruction. The tape system must be working somewhere near the correct speed, but this test will work over wide limits of tape-speed error. There is no cumulative error as the tape sweeps from one end to the other. The program performs a CHK i instruction and then waits 1.024 milliseconds, and samples the IBZ instruction. The tape should be in the middle of an interblock zone. If not, the tape is stopped at block 60, and the computer halts at 471. If no error occurs, the program executes a 2.048 millisecond delay to get out the interblock zone; and tests the IBZ instruction again. This process is continued for even blocks from block 0 to block 402.

TEST #62 JMPUP

This is a test of the JMP instruction. The program saves the control program in quarter 4 and then executes JMP instructions to memory locations from 560 to 1777 and from 3 to 377. The error halts at location 472 recognizes an improper JMP instruction in register 0. The instruction which should be in 0 is in the ACCUMULATOR. A halt at any other location indicates that the most recent JMP instruction did not set the P register properly.

TEST #63 JMPDWN

This second JMP test executes JMP instructions to memory locations from 755 to 1777 and from 3 to 577.

The error halt at 667 indicates that an improper JMP instruction is in register 0. The proper JMP is in the ACCUMULATOR.

A halt at any location other than 667 indicates that a JMP instruction did not set the P register properly.

TEST #64 TAPETS

This is a general exercise of the magnetic tape instructions and tape unit 0. A "count by 11" test pattern is written on tape and then read back and checked word for word. The checksum and transfer checks are tested, and the tape working area is cleared before the test finishes. If a failure occurs during this test, the fault may lie either in the tape unit or the tape itself.

TEST #65 MTBTST

This test program checks the MTB instruction and the tape motion. The tape is set into motion with an MTB i instruction, and the machine goes into a long delay loop. If the tape speed is too slow, or if noise stops the tape motion, or if MTB does not put the proper code in the ACCUMULATOR; the program will indicate an error. The tape is moved in both directions and should continue moving during the entire time that the machine is executing the delay loop.

TEST #66 DISTST

TEST #67 DSCTST

The programs DISTST and DSCTST are not test programs in the usual sense, since no error halts are included in the programs. These programs

exercise the DIS and DSC instructions, and patterns will be displayed on the LINC display oscilloscope.

If the machine hangs up in one of these programs, a malfunction is indicated in one of the display instructions.

TEST #700 OVFT1

This is a test of the SKP14 or OVF instruction. Various patterns of positive and negative numbers are added, and the overflow flip-flop is checked after each addition.

TEST #701 ZTAT1

This is a test of the MSC5 or ZTA instruction. The test transfers numbers from 0 - 3777 from A to Z, and then back from Z to A. Since Z_{11} transfers into A_{10}, the original number is scaled right by 1 bit before it is compared to the transferred number.

TEST #702 ZCLR1

Only a few instructions should clear the Z register. All the order code instructions which should not clear the Z register are executed by this test. If the given number pattern in Z is changed by the instruction tested, an error is indicated.

TEST #703 ZCLRT2

KNOB 0 must be turned fully clockwise.

Various number patterns are loaded into the Z register and then a SAM 0 instruction is executed. If the SAM 0 does not get 177, an error is indicated. The error could be caused by improper clearing of Z, or by trouble in the analog inputs.

PROGRAM #705 ENIT1

This test program exercises the interrupt function. The control program is saved in QN 4, and most of the lower memory is cleared. Since nothing is connected to the interrupt request line, the computer will interrupt on every instruction following ENI except a JMP.

Several conditions of interrupt and no interrupt are checked with a PIN instruction. An error in either the ENI or PIN instructions will cause the computer to halt, or to hang up in a pause.

TEST #71 MISCTS

This test program exercises a few instructions which are not used in previous tests. The instructions tested are SNS, SXL, KST, RSW, and LSW. If the machine halts during this test, the instruction immediately preceding the halt is suspect. The switches on the console must be set as follows for the program to run properly: RIGHT SWITCHES, 0300; LEFT SWITCHES, 0700; SENSE SWITCHES, 77.

TEST #4002 GETLEP
NO NUMBER LPFROG

GETLEP (get leap frog) is a program that reads LPFROG (leap frog) into quarter 0 and then jumps to 20. This is necessary because LPFROG was initially written that way and for historical and other reasons was not changed to run in quarter 1.

LPFROG takes its name from the fact that it moves itself through memory. The program does only three things. First, it moves itself to a new area in memory. The new starting location is the old starting location, plus the constant on the RIGHT SWITCHES. Second, the program performs a checksum on the relocated program. The result, in the ACCUMULATOR, should be -0. Third, if the checksum is correct the program jumps to the new starting address and the process is repeated.

If, after relocation, the program will exceed 1777, the new starting address is set to 20 plus the amount that the program would have exceeded 1777. In this way, many different starting locations are generated. The increment on the RIGHT SWITCHES must be at least as big as the length of the program (101) and no larger than 1777 minus twice the length of the program minus 17 (1556).

The purpose of LPFROG is to exercise the computer. If a failure should occur, however, it is extremely difficult to find out what has happened. To further complicate the matter, LPFROG cannot, in general, be restarted in any way after an error halt. It may be possible to restart at the present starting address, contents of 1, but the best approach is to read it into quarter 0 from tape and START 20. It may be possible to determine in general what has failed, but since LPFROG cannot be cycled in a given area, this may not be of too much help. If any of the other tests indicate an error, use them to try to find out what is wrong.

LPFROG is extremely sensitive to the adjustment of MDEL 2. Failure of LPFROG probably indicates some sort of memory trouble, so this should be the first area to check. If only LPFROG will fail, the best advice is to refer to its manuscript and to try to learn from that which has happened. Please remember that LPFROG is not intended to be a diagnostic tool.

LINC Volume 15

Assembly and Test Procedures

Section 3

INDEX TO TEST TAPE

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INDEX TO TEST TAPE

Contents

INDEX TO TEST TAPE

Introduction

The following is an index of the test tape. It contains the central logic test programs, the test and adjustment programs, and their manuscripts. The index is ordered by the tape block number which contains the information. The manuscript files are those created by the LAP IV manuscript control meta command.

1. Central Logic Test Programs

BLOCK	TITLE	PROGRAM NUMBER
0	CONTRL	
1	HLTTST	70
2	SAETST	1
3	BCLTST	2
4	BSETST	3
5	BCOTST	4
6	ROLT1	5
7	ROLT2	6
10	ROLT3	7
11	ROLT4	10
12	ROLT5	11
13	RORT1	12
14	RORT2	13
15	RORT3	14
16	RORT4	15
17	RORT5	16
20	CLRTST	17
21	ADDONE	20
22	COMT1	21
23	SCRT1	22
24	SCRT2	23

BLOCK	TITLE	PROGRAM NUMBER
25	SCRT3	24
26		
27	SCRT4	25
30		
31	ADDT1	26
32	FADRT1	27
33	FADRT2	30
34		
35	iBETA1	31
36	iBETA2	32
37	iBETA3	33
40	iBETA4	34
41	LDAT1	35
42	STAT1	36
43	ADMT1	37
44	LAMT1	40
45	MULT1	41
46	SROT1	42
47	SETT1	43
50	SETT2	44
51	XSKT1	45
52	XSKT2	46
53	AZET1	47
54	APOT1	50
55	LZET1	51

BLOCK	TITLE	PROGRAM NUMBER
56	HWCT1	52
57	HWCT2	53
60	HWCT3	54
61	HWCT4	55
62	HWCT5	56
63	RANADD	57
64	ATRT1	60
65	IBZT1	61
66	JMPUP	62
67	JMPDWN	63
70	TAPE TS	64
71		
72		
73	WORKING AREA	
74	FOR TAPE TEST	
75		
76		
77		
100		
101	MTBTST	65
102	DISTST	66
103	DSCTST	67
104	OVFT1	700
105	ZTAT1	701

BLOCK	TITLE	PROGRAM NUMBER
106	ZCLR1	702
107	ZCLRT2	703
110	ENIT1	704
111	MISCTS	71
112	GETLEP	4002
113	LPFROG	----

2. Test and Adjustment Programs

BLOCK	TITLE		START LOCATION
200	Keyboard Test One	(KBDTS1)	20
201			
202	Keyboard Test Two	(KBDTS2)	400
203			
204	Square	(SQUARE)	400
205	Magnetic Tape Test	(MTPTST)	20
206	Toggle Test One	(SNST1)	20
207	Toggle Test Two	(RSWT1)	20
210	Toggle Test Three	(LSWT1)	20
211	Ladder One	(XLADER)	20
212	Ladder Two	(YLADER)	20
213	Relay Check	(RELCHi)	400
214			
215	0 Set	(0 SET)	20
216	Anacal	(ANACAL)	20
217	Memory Test One	(MEMTST)	20
220	Memory Test Two		400
221	Knobs	(KNOBS)	20
222			
223	Mark	(MARK)	20

3. Program Manuscripts - File 3

NAME	BLOCK
GETLEP	301
CONTRL	303
LPFROG	305
iBETA1	307
iBETA2	311
iBETA3	313
iBETA4	316
LDAT1	321
STAT1	323
ADMT1	325
LAMT1	327
MULT1	331
SROT1	334
SETT1	336
SETT2	340
XSKT1	342
XSKT2	345
AZET1	350
APOT1	352
LZET1	354
HWCT1	356

NAME	BLOCK
HWCT2	361
HWCT3	363
HWCT4	366
HWCT5	371
RANADD	375

4. Program Manuscripts - File 4

NAME	BLOCK
KBDTS1	401
KBDTS2	411
ATRT1	416
IBZT1	420
JMPUP	422
JMPDWN	425
ZTAT1	430
ZCLRT1	433
ZCLRT2	436
ENIT1	440
WRCTST	443
OVFT1	445
SQUARE	451
MTPTST	454
SNST1	460
RSWT1	462
LSWT1	464
XLADER	466
YLADER	470
0 SET	472
MEMTST	474

5. Program Manuscripts - File 5

NAME	BLOCK
RELCK1	501
ANACAL	511
KNOBS	515
MARK	520
CONTRL	525
SAETST	527
BCLTST	532
BSETST	535
BCOTST	540
ROLT1	543
ROLT2	545
ROLT3	547
ROLT4	551
ROLT5	553
RORT1	555
RORT2	557
RORT3	561
RORT4	563
RORT5	565
CLRTST	567
ADDONE	571
COMT1	573
SCRT1	575

6. Program Manuscripts - File 6

NAME	BLOCK
SCRT2	601
SCRT3	605
SCRT4	611
ADDT1	616
FADRT1	620
FADRT2	622
DSCTST	625
DISTST	627
MTBTST	632
HLTTST	634
TAPETS	636
MISCTS	643

```
                0001    [CONTRL
                0002    [CONTROL PROG
                0003    ⊟20
0020    0020    0004    #1R RDC         0700    Read program
0021    0021    0005        111         1001
0022    0022    0006        JMP 401     6401    To test program
0023    0023    0007    #1A CLR         0011
0024    0024    0010        BSE i       1620
0025    0025    0011        111         1001    Set BN = 1 and QN = 1
0026    0026    0012        STC 1R+1    4021
0027    0027    0013    #1S CLR         0011
0030    0030    0014        BSE i       1620
0031    0031    0015        1           0001    Set increment = 1
0032    0032    0016        STC 1I      4046
0033    0033    0017        JMP 1R      6020    To tape read
0034    0034    0020    #1T LDA         1000
0035    0035    0021        1R+1        0021
0036    0036    0022        ADD 1I      2046    Read next test
0037    0037    0023        STC 1R+1    4021
0040    0040    0024        JMP 1S      6027
0041    0041    0025    #1B LSW         0517
0042    0042    0026        BSE i       1620
0043    0043    0027        110         1000    Read specified block
0044    0044    0030        STC 1R+1    4021
0045    0045    0031        JMP 1S      6027
0046    0046    0032    #1I 1           0001    Increment
0047    0047    0033    #1V 1002        1002
```

```
          0001      [HLTTST
          0002      ⊟400
0400      0003           70              0070
0401      0004           HLT             0000
0402      0005           JMP 34          6034
          0006      [IF MACHINE
          0007      [DOES NOT HALT
          0010      [AT 401, THE
          0011      [FOLLOWING
          0012      [TESTS ARE
          0013      [MEANINGLESS.
          0014      [
          0015      [
          0016      [RAISE THE
          0017      [RESUME LEVER
          0020      [TO CONTINUE
```

```
0001      [SAETST
0002      [SAE TEST
0003      ⊟400
0400 0004       1                    0001  Program number
0401 0005  #2S  SET i 1              0061
0402 0006       7677                 7677
0403 0007  ┌#2A LDA i                1020
0404 0010  │    0                    0000
0405 0011  │    SAE i                1460
0406 0012  └    0                    0000
0407 0013       HLT                  0000  Error. ACC = 0000; Y = 0000
0410 0014  ┌    LDA i                1020
0411 0015  │    7777                 7777
0412 0016  │    SAE i                1460
0413 0017  │    7777                 7777
0414 0020  └    HLT                  0000  Error. ACC = 7777; Y = 7777
0415 0021  ┌    LDA i                1020
0416 0022  │    0                    0000
0417 0023  │    SAE i                1460
0420 0024  └    7777                 7777
0421 0025       JMP P+2              6423
0422 0026       HLT                  0000  Error. ACC = 0000; Y = 7777
0423 0027  ┌    LDA i                1020
0424 0030  │    7777                 7777
0425 0031  │    SAE i                1460
0426 0032  └    0                    0000
0427 0033       JMP P+2              6431
0430 0034       HLT                  0000  Error. ACC = 7777; Y = 0000
0431 0035       SET i 2              0062
0432 0036       7763                 7763
0433 0037       SET i 3              0063
0434 0040       3A-1                 0505
0435 0041  ┌#2B LDA i 3              1023
0436 0042  └    SAE 3                1443
0437 0043       HLT                  0000  Error. ACC = Float 0; Y = Float o
0440 0044       XSK i 2              0222  Finish 14 patterns ?
0441 0045       JMP 2B               6435
0442 0046       SET i 2              0062
0443 0047       7763                 7763
0444 0050       SET i 3              0063
0445 0051       3B-1                 0521
0446 0052  ┌#2C LDA i 3              1023
0447 0053  └    SAE 3                1443
0450 0054       HLT                  0000  Error. ACC = Float 1; Y = Float 1
0451 0055       XSK i 2              0222  Finish 14 patterns ?
0452 0056       JMP 2C               6446
0453 0057       SET i 2              0062
0454 0060       7763                 7763
0455 0061       SET i 3              0063
0456 0062       3A-1                 0505
0457 0063       SET i 4              0064
0460 0064       3B-1                 0521
0461 0065  ┌#2D LDA i 3              1023
0462 0066  └    SAE i 4              1464
0463 0067       JMP P+2              6465
0464 0070       HLT                  0000  Error. ACC = Float 0; Y = Float 1
0465 0071       XSK i 2              0222  Finish 14 patterns ?
0466 0072       JMP 2D               6461
0467 0073       SET i 2              0062
0470 0074       7763                 7763
0471 0075       SET i 3              0063
0472 0076       3B-1                 0521
0473 0077       SET i 4              0064
```

```
0474  0100          3A-1                  0505   [SAETST                4
0475  0101  [#2E LDA i 3                  1023
0476  0102   [    SAE i 4                  1464
0477  0103        JMP P+2                 6501
0500  0104        HLT                     0000   Error. ACC = Float 1; Y = Float 0
0501  0105        XSK i 2                 0222   Finish 12 patterns ?
0502  0106        JMP 2E                  6475   NO
0503  0107        XSK i 1                 0221   Finish test 100 times ?
0504  0110        JMP 2A                  6403   NO
0505  0111        JMP 1T                  6034   YES
0506  0112   #3A  7776                    7776]
0507  0113        7775                    7775|
0510  0114        7773                    7773|
0511  0115        7767                    7767|
0512  0116        7757                    7757|
0513  0117        7737                    7737|  Float 0 pattern
0514  0120        7677                    7677|
0515  0121        7577                    7577|
0516  0122        7377                    7377|
0517  0123        6777                    6777|
0520  0124        5777                    5777|
0521  0125        3777                    3777]
0522  0126   #3B  0001                    0001]
0523  0127        0002                    0002|
0524  0130        0004                    0004|
0525  0131        0010                    0010|
0526  0132        0020                    0020|
0527  0133        0040                    0040|
0530  0134        0100                    0100|
0531  0135        0200                    0200|  Float 1 pattern
0532  0136        0400                    0400|
0533  0137        1000                    1000|
0534  0140        2000                    2000|
0535  0141        4000                    4000]
```

```
                0001    [BCLTST
                0002    [BCL TEST
                0003    @400
0400            0004        2                   0002    Test number
0401            0005    #2S SET i 1             0061    Do test 40 times
0402            0006        7737                7737
0403            0007    #2A LDA i               1020
0404            0010        0                   0000
0405            0011        BCL i               1560
0406            0012        0                   0000
0407            0013        SAE i               1460
0410            0014        0                   0000
0411            0015        HLT                 0000    Error. ACC = 0; Y = 0; Result = 0
0412            0016        LDA i               1020
0413            0017        7777                7777
0414            0020        BCL i               1560
0415            0021        7777                7777
0416            0022        SAE i               1460
0417            0023        0                   0000
0420            0024        HLT                 0000    Error. ACC = 7777; Y = 7777;
0421            0025        LDA i               1020    Result = 0
0422            0026        0                   0000
0423            0027        BCL i               1560
0424            0030        7777                7777
0425            0031        SAE i               1460
0426            0032        0                   0000
0427            0033        HLT                 0000    Error. ACC = 0; Y = 7777;
0430            0034        LDA i               1020    Result = 0
0431            0035        7777                7777
0432            0036        BCL i               1560
0433            0037        0                   0000
0434            0040        SAE i               1460
0435            0041        7777                7777
0436            0042        HLT                 0000    Error. ACC = 7777; Y = 0;
0437            0043        SET i 2             0062    Result = 7777
0440            0044        7763                7763
0441            0045        SET i 3             0063
0442            0046        3B-1                0537
0443            0047        SET i 4             0064
0444            0050        3A-1                0523
0445            0051    #2B LDA i               1020
0446            0052        7777                7777
0447            0053        BCL i 3             1563
0450            0054        SAE i 4             1464
0451            0055        HLT                 0000    Error. ACC = 7777; Y = Float 1;
0452            0056        XSK i 2             0222    Result = Float 0
0453            0057        JMP 2B              6445
0454            0060        SET i 2             0062
0455            0061        7763                7763
0456            0062        SET i 3             0063
0457            0063        3A-1                0523
0460            0064        SET i 4             0064
0461            0065        3B-1                0537
0462            0066    #2C LDA i               1020
0463            0067        7777                7777
0464            0070        BCL i 3             1563
0465            0071        SAE i 4             1464
0466            0072        HLT                 0000    Error. ACC = 7777; Y = Float 0;
0467            0073        XSK i 2             0222    Result = Float 1
0470            0074        JMP 2C              6462
0471            0075        SET i 2             0062
0472            0076        7763                7763
0473            0077        SET i 3             0063
```

```
0474  0100        3B-1          0537   [BCLTST
0475  0101  #2D   LDA i          1020
0476  0102        0             0000
0477  0103        BCL i 3       1563
0500  0104        SAE i         1460
0501  0105        0             0000
0502  0106        HLT           0000   Error. ACC = 0; Y = Float 1;
0503  0107        XSK i 2       0222   Result = 0
0504  0110        JMP 2D        6475
0505  0111        SET i 2       0062
0506  0112        7763          7763
0507  0113        SET i 3       0063
0510  0114        3A-1          0523
0511  0115  #2E   LDA i          1020
0512  0116        0             0000
0513  0117        BCL i 3       1563
0514  0120        SAE i         1460
0515  0121        0             0000
0516  0122        HLT           0000   Error. ACC = 0; Y = Float 0;
0517  0123        XSK i 2       0222   Result = 0
0520  0124        JMP 2E        6511
0521  0125        XSK i 1       0221
0522  0126        JMP 2A        6403
0523  0127        JMP 1T        6034   Read next test
0524  0130  #3A   7776          7776
0525  0131        7775          7775
0526  0132        7773          7773
0527  0133        7767          7767
0530  0134        7757          7757
0531  0135        7737          7737   Float 0
0532  0136        7677          7677
0533  0137        7577          7577
0534  0140        7377          7377
0535  0141        6777          6777
0536  0142        5777          5777
0537  0143        3777          3777
0540  0144  #3B   1             0001
0541  0145        2             0002
0542  0146        4             0004
0543  0147        10            0010
0544  0150        20            0020
0545  0151        40            0040
0546  0152        100           0100   Float 1
0547  0153        200           0200
0550  0154        400           0400
0551  0155        1000          1000
0552  0156        2000          2000
0553  0157        4000          4000
```

```
                0001    [BSETST
                0002    [BSE TEST
                0003    @400
0400    0004            3                       0003    Test number
0401    0005    #2S     SET i 1                 0061    Do test 40 times
0402    0006            7737                    7737
0403    0007    [#2A    LDA i                   1020
0404    0010    |       00                      0000
0405    0011    |       BSE i                   1620
0406    0012    [       0                       0000
0407    0013            SAE i                   1460
0410    0014            0                       0000
0411    0015            HLT                     0000    Error. ACC = 0; Y = 0; Result = 0
0412    0016        [   LDA i                   1020
0413    0017        |   7777                    7777
0414    0020        |   BSE i                   1620
0415    0021        [   7777                    7777
0416    0022            SAE i                   1460
0417    0023            7777                    7777
0420    0024            HLT                     0000    Error. ACC = 7777; Y = 7777;
0421    0025        [   LDA i                   1020    Result = 7777
0422    0026        |   0                       0000
0423    0027        |   BSE i                   1620
0424    0030        [   7777                    7777
0425    0031            SAE i                   1460
0426    0032            7777                    7777
0427    0033            HLT                     0000    Error. ACC = 0; Y = 7777;
0430    0034        [   LDA i                   1020    Result = 7777
0431    0035        |   7777                    7777
0432    0036        |   BSE i                   1620
0433    0037        [   0                       0000
0434    0040            SAE i                   1460
0435    0041            7777                    7777
0436    0042            HLT                     0000    Error. ACC = 7777; Y = 0;
0437    0043            SET i 2                 0062    Result = 7777
0440    0044            7763                    7763
0441    0045            SET i 3                 0063
0442    0046            3B-1                    0533
0443    0047    [#2B    LDA i                   1020
0444    0050    |       0                       0000
0445    0051    [       BSE i 3                 1623
0446    0052            SAE 3                   1443
0447    0053            HLT                     0000    Error. ACC = 0; Y = Float 1;
0450    0054            XSK i 2                 0222    Result = Float 1
0451    0055            JMP 2B                  6443
0452    0056            SET i 2                 0062
0453    0057            7763                    7763
0454    0060            SET i 3                 0063
0455    0061            3A-1                    0517
0456    0062    [#2C    LDA i                   1020
0457    0063    |       0                       0000
0460    0064    [       BSE i 3                 1623
0461    0065            SAE 3                   1443
0462    0066            HLT                     0000    Error. ACC = 0; Y = Float 0;
0463    0067            XSK i 2                 0222    Result = Float 0
0464    0070            JMP 2C                  6456
0465    0071            SET i 2                 0062
0466    0072            7763                    7763
0467    0073            SET i 3                 0063
0470    0074            3B-1                    0533
0471    0075    [#2D    LDA i                   1020
0472    0076    |       7777                    7777
0473    0077    [       BSE i 3                 1623
```

```
0474  0100          SAE i          1460
0475  0101          7777           7777
0476  0102          HLT            0000   Error. ACC = 7777; Y = Float 1;
0477  0103          XSK i 2        0222   Result = 7777
0500  0104          JMP 2D         6471
0501  0105          SET i 2        0062
0502  0106          7763           7763
0503  0107          SET i 3        0063
0504  0110          3A-1           0517
0505  0111  #2E LDA i              1020
0506  0112          7777           7777
0507  0113          BSE i 3        1623
0510  0114          SAE i          1460
0511  0115          7777           7777
0512  0116          HLT            0000   Error. ACC = 7777; Y = Float 0;
0513  0117          XSK i 2        0222   Result = 7777
0514  0120          JMP 2E         6505
0515  0121          XSK i 1        0221
0516  0122          JMP 2A         6403
0517  0123          JMP 1T         6034   To read next test
0520  0124    #3A   7776           7776
0521  0125          7775           7775
0522  0126          7773           7773
0523  0127          7767           7767
0524  0130          7757           7757
0525  0131          7737           7737   Float 0
0526  0132          7677           7677
0527  0133          7577           7577
0530  0134          7377           7377
0531  0135          6777           6777
0532  0136          5777           5777
0533  0137          3777           3777
0534  0140    #3B   1              0001
0535  0141          2              0002
0536  0142          4              0004
0537  0143          10             0010
0540  0144          20             0020
0541  0145          40             0040
0542  0146          100            0100   Float 1
0543  0147          200            0200
0544  0150          400            0400
0545  0151          1000           1000
0546  0152          2000           2000
0547  0153          4000           4000
```

```
                0001    [BCOTST
                0002    [BCO TEST
                0003    @400
0400            0004        4                       0004  Test number
0401            0005    #2S SET i 1                 0061
0402            0006        7737                    7737
0403            0007    [#2A LDA i                  1020
0404            0010    [   0                       0000
0405            0011    [   BCO i                   1660
0406            0012    [   0                       0000
0407            0013        SAE i                   1460
0410            0014        0                       0000
0411            0015        HLT                     0000  Error. ACC = 0; Y = 0; Result = 0
0412            0016        [LDA i                  1020
0413            0017        [7777                   7777
0414            0020        [BCO i                  1660
0415            0021        [7777                   7777
0416            0022        SAE i                   1460
0417            0023        0                       0000
0420            0024        HLT                     0000  Error. ACC = 7777; Y = 7777;
0421            0025        [LDA i                  1020  Result = 0
0422            0026        [0                      0000
0423            0027        [BCO i                  1660
0424            0030        [7777                   7777
0425            0031        SAE i                   1460
0426            0032        7777                    7777
0427            0033        HLT                     0000  Error. ACC = 0; Y = 7777;
0430            0034        [LDA i                  1020  Result = 7777
0431            0035        [7777                   7777
0432            0036        [BCO i                  1660
0433            0037        [0                      0000
0434            0040        SAE i                   1460
0435            0041        7777                    7777
0436            0042        HLT                     0000  Error. ACC = 7777; Y = 0;
0437            0043        SET i 2                 0062  Result = 7777
0440            0044        7763                    7763
0441            0045        SET i 3                 0063
0442            0046        3B-1                    0535
0443            0047        SET i 4                 0064
0444            0050        3A-1                    0521
0445            0051    [#2B LDA i                  1020
0446            0052    [   7777                    7777
0447            0053    [   BCO i 3                 1663
0450            0054        SAE i 4                 1464
0451            0055        HLT                     0000  Error. ACC = 7777; Y = Float 1;
0452            0056        XSK i 2                 0222  Result = Float 0
0453            0057        JMP 2B                  6445
0454            0060        SET i 2                 0062
0455            0061        7763                    7763
0456            0062        SET i 3                 0063
0457            0063        3A-1                    0521
0460            0064        SET i 4                 0064
0461            0065        3B-1                    0535
0462            0066    [#2C LDA i                  1020
0463            0067    [   7777                    7777
0464            0070    [   BCO i 3                 1663
0465            0071        SAE i 4                 1464
0466            0072        HLT                     0000  Error. ACC = 7777; Y = Float 0;
0467            0073        XSK i 2                 0222  Result = Float 1
0470            0074        JMP 2C                  6462
0471            0075        SET i 2                 0062
0472            0076        7763                    7763
0473            0077        SET i 3                 0063
```

```
0474  0100          3B-1                0535  [BCOTST
0475  0101  [#2D LDA i                  1020
0476  0102  [      0                    0000
0477  0103  [      BCO i 3              1663
0500  0104          SAE 3               1443
0501  0105          HLT                 0000  Error. ACC = 0; Y = Float 1;
0502  0106          XSK i 2             0222  Result = Float 1
0503  0107          JMP 2D              6475
0504  0110          SET i 2             0062
0505  0111          7763                7763
0506  0112          SET i 3             0063
0507  0113          3A-1                0521
0510  0114  [#2E LDA i                  1020
0511  0115  [      0                    0000
0512  0116  [      BCO i 3              1663
0513  0117          SAE 3               1443
0514  0120          HLT                 0000  Error. ACC = 0; Y = Float 0;
0515  0121          XSK i 2             0222  Result = Float 0
0516  0122          JMP 2E              6510
0517  0123          XSK i 1             0221
0520  0124          JMP 2A              6403
0521  0125          JMP 1T              6034  To next test
0522  0126    #3A   7776                7776
0523  0127          7775                7775
0524  0130          7773                7773
0525  0131          7767                7767
0526  0132          7757                7757
0527  0133          7737                7737  Float 0
0530  0134          7677                7677
0531  0135          7577                7577
0532  0136          7377                7377
0533  0137          6777                6777
0534  0140          5777                5777
0535  0141          3777                3777
0536  0142    #3B   1                   0001
0537  0143          2                   0002
0540  0144          4                   0004
0541  0145          10                  0010
0542  0146          20                  0020
0543  0147          40                  0040
0544  0150          100                 0100  Float 1
0545  0151          200                 0200
0546  0152          400                 0400
0547  0153          1000                1000
0550  0154          2000                2000
0551  0155          4000                4000
```

```
                0001    [ROLT1
                0002    [ROL TEST 1
                0003    [FLOAT 1
                0004    [i=0
                0005    ⊟400
0400            0006        S                   0005  Test number
0401            0007    #2S SET i 1             0061  Do test 10 times
0402            0010        7767                7767
0403            0011    #2A SET i 3             0063  Do 14 patterns
0404            0012        7763                7763
0405            0013        SET i 4             0064  Set test constant address
0406            0014        2T-1                0447
0407            0015    #2B SET i 5             0065  Shift count
0410            0016        0                   0000
0411            0017        SET i 6             0066  Do 20 counts  0 - 17
0412            0020        7757                7757
0413            0021        XSK i 4             0224
0414            0022    #2C LDA                 1000
0415            0023        2R                  0433
0416            0024        BCL i               1560  Clear count bits
0417            0025        17                  0017
0420            0026        STC 2R              4433
0421            0027        LDA                 1000
0422            0030        2R                  0433
0423            0031        BSE                 1600  Set shift count
0424            0032        5                   0005
0425            0033        STC 2R              4433
0426            0034        ADD 4               2004  Compute address of test result
0427            0035        ADD 5               2005
0430            0036        STC 7               4007
0431            0037        CLR                 0011  Clear line bit
0432            0040        LDA 4               1004  Load test constant
0433            0041    #2R ROL                 0240  Do rotate
0434            0042        SAE 7               1447
0435            0043        HLT                 0000  Error in ACC
0436            0044        LZE                 0452
0437            0045        HLT                 0000  Error. Link bit ≠ 0
0440            0046        XSK i 5             0225
0441            0047        XSK i 6             0226
0442            0050        JMP 2C              6414
0443            0051        XSK i 3             0223
0444            0052        JMP 2B              6407
0445            0053        XSK i 1             0221
0446            0054        JMP 2A              6403
0447            0055        JMP 1T              6034
0450            0056    #2T 1                   0001
0451            0057        2                   0002
0452            0060        4                   0004
0453            0061        10                  0010
0454            0062        20                  0020
0455            0063        40                  0040
0456            0064        100                 0100
0457            0065        200                 0200
0460            0066        400                 0400
0461            0067        1000                1000
0462            0070        2000                2000
0463            0071        4000                4000
0464            0072        1                   0001
0465            0073        2                   0002
0466            0074        4                   0004
0467            0075        10                  0010
0470            0076        20                  0020
0471            0077        40                  0040
```

```
0472    0100    100     0100    [ROLT1
0473    0101    200     0200
0474    0102    400     0400
0475    0103    1000    1000
0476    0104    2000    2000
0477    0105    4000    4000
0500    0106    1       0001
0501    0107    2       0002
0502    0110    4       0004
0503    0111    10      0010
```

```
                0001    [ROLT2
                0002    [ROL TEST 2
                0003    [FLOAT 0
                0004    [i=0
                0005    ⊟400
0400            0006        6                   0006    Test number
0401            0007    #2S SET i 1             0061 ]  Do test 10 times
0402            0010        7767                7767 ]
0403            0011    #2A SET i 3             0063 ]  Do 14 patterns
0404            0012        7763                7763 ]
0405            0013        SET i 4             0064 ]  Set test constant address
0406            0014        2T-1                0451 ]
0407            0015    #2B SET i 5             0065 ]  Shift count
0410            0016        0                   0000 ]
0411            0017        SET i 6             0066 ]  Do 20 counts, 0 - 17
0412            0020        7757                7757 ]
0413            0021        XSK i 4             0224 |
0414            0022    #2C LDA                 1000 ]
0415            0023        2R                  0435 |
0416            0024        BCL i               1560 |  Clear count bits in ROL
0417            0025        17                  0017 |
0420            0026        STC 2R              4435 ]
0421            0027        LDA                 1000 ]
0422            0030        2R                  0435 |
0423            0031        BSE                 1600 |  Set shift count bits in ROL
0424            0032        5                   0005 |
0425            0033        STC 2R              4435 ]
0426            0034        ADD 4               2004 ]
0427            0035        ADD 5               2005 |  Compute address of test result
0430            0036    [   STC 7               4007 ]
0431            0037    |   LDA i               1020 ]
0432            0040    |   4000                4000 |  Set link bit
0433            0041    |   ROL i 1             0261 ]
0434            0042    |   LDA 4               1004
0435            0043    [#2R ROL                0240
0436            0044        SAE 7               1447
0437            0045        HLT                 0000    Error. ACC
0440            0046        LZE i               0472
0441            0047        HLT                 0000    Error. Link bit ≠ 1
0442            0050        XSK i 5             0225
0443            0051        XSK i 6             0226
0444            0052        JMP 2C              6414
0445            0053        XSK i 3             0223
0446            0054        JMP 2B              6407
0447            0055        XSK i 1             0221
0450            0056        JMP 2A              6403
0451            0057        JMP 1T              6034
0452            0060    #2T 7776                7776
0453            0061        7775                7775
0454            0062        7773                7773
0455            0063        7767                7767
0456            0064        7757                7757
0457            0065        7737                7737
0460            0066        7677                7677
0461            0067        7577                7577
0462            0070        7377                7377
0463            0071        6777                6777
0464            0072        5777                5777
0465            0073        3777                3777
0466            0074        7776                7776
0467            0075        7775                7775
0470            0076        7773                7773
0471            0077        7767                7767
```

```
0472    0100    7757    7757    [ROLT2
0473    0101    7737    7737
0474    0102    7677    7677
0475    0103    7577    7577
0476    0104    7377    7377
0477    0105    6777    6777
0500    0106    5777    5777
0501    0107    3777    3777
0502    0110    7776    7776
0503    0111    7775    7775
0504    0112    7773    7773
0505    0113    7767    7767
```

```
                0001    [ROLT3
                0002    [ROL TEST 3
                0003    [FLOAT 1
                0004    [i=1
                0005    =400
0400            0006        7                   0007    Test number
0401            0007    #2S SET i 1             0061    Do test 10 times
0402            0010        7767                7767
0403            0011    #2A SET i 3             0063    Do 14 patterns
0404            0012        7763                7763
0405            0013        SET i 4             0064    Set test constant address
0406            0014        2T-1                0445
0407            0015    #2B SET i 5             0065    Shift count
0410            0016        0                   0000
0411            0017        SET i 6             0066    Do 20 counts, 0 - 17
0412            0020        7757                7757
0413            0021        XSK i 4             0224
0414            0022    #2C LDA                 1000
0415            0023        2R                  0433
0416            0024        BCL i               1560    Clear count bits
0417            0025        17                  0017
0420            0026        STC 2R              4433
0421            0027        LDA                 1000
0422            0030        2R                  0433
0423            0031        BSE                 1600    Set shift count bits in ROL
0424            0032        5                   0005
0425            0033        STC 2R              4433
0426            0034        ADD 4               2004
0427            0035        ADD 5               2005    Compute address of test result
0430            0036        STC 7               4007
0431            0037        CLR                 0011    Clear link bit
0432            0040        LDA 4               1004
0433            0041    #2R ROL i               0260
0434            0042        SAE 7               1447
0435            0043        HLT                 0000    Error.
0436            0044        XSK i 5             0225
0437            0045        XSK i 6             0226
0440            0046        JMP 2C              6414
0441            0047        XSK i 3             0223
0442            0050        JMP 2B              6407
0443            0051        XSK i 1             0221
0444            0052        JMP 2A              6403
0445            0053        JMP 1T              6034
0446            0054    #2T 1                   0001
0447            0055        2                   0002
0450            0056        4                   0004
0451            0057        10                  0010
0452            0060        20                  0020
0453            0061        40                  0040
0454            0062        100                 0100
0455            0063        200                 0200
0456            0064        400                 0400
0457            0065        1000                1000
0460            0066        2000                2000
0461            0067        4000                4000
0462            0070        0                   0000
0463            0071        1                   0001
0464            0072        2                   0002
0465            0073        4                   0004
0466            0074        10                  0010
0467            0075        20                  0020
0470            0076        40                  0040
0471            0077        100                 0100
```

```
0472    0100    200     0200    [ROLT3
0473    0101    400     0400
0474    0102    1000    1000
0475    0103    2000    2000
0476    0104    4000    4000
0477    0105    0       0000
0500    0106    1       0001
0501    0107    2       0002
0502    0110    4       0004
```

```
                0001    [WRCTST
                0002    ⊟400
0400    0400    0003        64              0064
0401    0401    0004        SET i 1         0061
0402    0402    0005        7775            7775
0403    0403    0006        LDA i           1020    Set tape increment
0404    0404    0007        2               0002    for two blocks.
0405    0405    0010        STC 46          4046
0406    0406    0011    #1I LDA             1000
0407    0407    0012        21              0021
0410    0410    0013        ADA i           1120
0411    0411    0014        1001            1001    Write pattern in
0412    0412    0015        STA             1040    next consec. block.
0413    0413    0016        1D              0452
0414    0414    0017        STA             1040
0415    0415    0020        1H              0501
0416    0416    0021        ADA i           1120
0417    0417    0022        1000            1000
0420    0420    0023        STC 1E          4454
0421    0421    0024        CLR             0011    Generate pattern in
0422    0422    0025        STA i           1060    QN2.
0423    0423    0026    #1A                 0000
0424    0424    0027        SET i 2         0062
0425    0425    0030        -400            7377
0426    0426    0031        SET i 3         0063
0427    0427    0032        777             0777
0430    0430    0033    #1B LDA             1000
0431    0431    0034        1A              0423
0432    0432    0035        STA i 3         1063
0433    0433    0036        LDA i           1020
0434    0434    0037        20              0020
0435    0435    0040        ADM             1140
0436    0436    0041        1A              0423
0437    0437    0042        XSK i 2         0222
0440    0440    0043        JMP 1B          6430
0441    0441    0044        SET i 2         0062    Clear out QN3.
0442    0442    0045        -400            7377
0443    0443    0046        SET i 3         0063
0444    0444    0047        1377            1377
0445    0445    0050        CLR             0011
0446    0446    0051    #1C STA i 3         1063
0447    0447    0052        XSK i 2         0222
0450    0450    0053        JMP 1C          6446
0451    0451    0054        WRC             0704
0452    0452    0055    #1D                 0000 — QN2 onto tape.
0453    0453    0056        RDC             0700
0454    0454    0057    #1E                 0000 — Tape into QN3.
0455    0455    0060        SET i 2         0062
0456    0456    0061        777             0777
0457    0457    0062        SET i 3         0063
0460    0460    0063        1377            1377
0461    0461    0064        SET i 4         0064
0462    0462    0065        -400            7377
0463    0463    0066    #1F LDA i 2         1022
0464    0464    0067        SAE i 3         1463
0465    0465    0070        HLT             0000 — Write instruction
0466    0466    0071        XSK i 4         0224    failed.
0467    0467    0072        JMP 1F          6463
0470    0470    0073        SET i 2         0062
0471    0471    0074        777             0777
0472    0472    0075        SET i 3         0063
0473    0473    0076        -400            7377
0474    0474    0077        CLR             0011
```

```
0475    0100    #1G STA i 2         1062  [WRCTST
0476    0101        XSK i 3         0223
0477    0102        JMP 1G          6475  Clear out QN2.
0500    0103        WRC             0704
0501    0104    #1H                 0000 - Clear test block.
0502    0105        XSK i 1         0221
0503    0106        JMP 1I          6406
0504    0107        JMP 34          6034
```

```
                0001    [ROLT4
                0002    [ROL TEST 4
                0003    [FLOAT 0
                0004    [i=0
                0005    @400
0400            0006        10                  0010  Test number ------
0401            0007    #2S SET i 1             0061  ]Do test 10 times
0402            0010        7767                7767  ]
0403            0011    #2A SET i 3             0063  ]Do 14 patterns
0404            0012        7763                7763  ]
0405            0013        SET i 4             0064  ]Set test constant address
0406            0014        2T-1                0447  ]
0407            0015    #2B SET i 5             0065  ]Shift count
0410            0016        0                   0000  ]
0411            0017        SET i 6             0066  ]Do 20 counts, 0 - 17
0412            0020        7757                7757  ]
0413            0021        XSK i 4             0224
0414            0022    #2C LDA                 1000  ]
0415            0023        2R                  0435  |
0416            0024        BCL i               1560  |Clear count bits
0417            0025        17                  0017  |
0420            0026        STC 2R              4435  ]
0421            0027        LDA                 1000  ]
0422            0030        2R                  0435  |
0423            0031        BSE                 1600  |Set shift count in ROL i
0424            0032        5                   0005  |
0425            0033        STC 2R              4435  ]
0426            0034        ADD 4               2004  ]
0427            0035        ADD 5               2005  |Compute address of test result
0430            0036        STC 7               4007  ]
0431            0037    [   LDA i               1020  ]
0432            0040    |   4000                4000  |Set link bit
0433            0041    |   ROL i 1             0261  ]
0434            0042    |   LDA 4               1004
0435            0043    [#2R ROL i              0260
0436            0044        SAE 7               1447
0437            0045        HLT                 0000  Error
0440            0046        XSK i 5             0225
0441            0047        XSK i 6             0226
0442            0050        JMP 2C              6414
0443            0051        XSK i 3             0223
0444            0052        JMP 2B              6407
0445            0053        XSK i 1             0221
0446            0054        JMP 2A              6403
0447            0055        JMP 1T              6034
0450            0056    #2T 7776                7776
0451            0057        7775                7775
0452            0060        7773                7773
0453            0061        7767                7767
0454            0062        7757                7757
0455            0063        7737                7737
0456            0064        7677                7677
0457            0065        7577                7577
0460            0066        7377                7377
0461            0067        6777                6777
0462            0070        5777                5777
0463            0071        3777                3777
0464            0072        7777                7777
0465            0073        7776                7776
0466            0074        7775                7775
0467            0075        7773                7773
0470            0076        7767                7767
0471            0077        7757                7757
```

```
0472    0100    7737    7737    [ROLT4
0473    0101    7677    7677
0474    0102    7577    7577
0475    0103    7377    7377
0476    0104    6777    6777
0477    0105    5777    5777
0500    0106    3777    3777
0501    0107    7777    7777
0502    0110    7776    7776
0503    0111    7775    7775
0504    0112    7773    7773
```

```
                0001    [ROLT5
                0002    [ROL TEST 5
                0003    [ALL 1 OR
                0004    [ALL 0
                0005    [i=0 OR
                0006    [i=1
                0007    ⊟400
0400    0400    0010        11                  0011    Test number
0401    0401    0011    #2S SET i 1             0061    Do test 10 times
0402    0402    0012        7767                7767
0403    0403    0013    #2A LDA i               1020
0404    0404    0014        ROL                 0240
0405    0405    0015        STA                 1040    Set up 2 ROL orders
0406    0406    0016        2R                  0422
0407    0407    0017        STC 3R              4435
0410    0410    0020        LDA i               1020
0411    0411    0021        ROL i               0260
0412    0412    0022        STA                 1040    Set up 2 ROL i orders
0413    0413    0023        4R                  0450
0414    0414    0024        STC 5R              4457
0415    0415    0025        SET i 2             0062    Do 20 counts, 0 - 17
0416    0416    0026        7757                7757
0417    0417    0027    #2B CLR                 0011    Clear link bit
0420    0420    0030        LDA i               1020
0421    0421    0031        7777                7777
0422    0422    0032    #2R 0                   0000    ROL order
0423    0423    0033        SAE i               1460
0424    0424    0034        7777                7777
0425    0425    0035        HLT                 0000    ACC error. ACC = 7777; i = 0
0426    0426    0036        LZE                 0452
0427    0427    0037        HLT                 0000    Error. Link bit ≠ 0
0430    0430    0040        LDA i               1020
0431    0431    0041        4000                4000
0432    0432    0042        ROL i 1             0261
0433    0433    0043        LDA i               1020
0434    0434    0044        0                   0000
0435    0435    0045    #3R 0                   0000    ROL order
0436    0436    0046        SAE i               1460
0437    0437    0047        0                   0000
0440    0440    0050        HLT                 0000    ACC error. ACC = 0; i = 0
0441    0441    0051        LZE i               0472
0442    0442    0052        HLT                 0000    Error. Link bit ≠ 1
0443    0443    0053        LDA i               1020
0444    0444    0054        4000                4000
0445    0445    0055        ROL i 1             0261
0446    0446    0056        LDA i               1020
0447    0447    0057        7777                7777
0450    0450    0060    #4R 0                   0000    ROL i order
0451    0451    0061        SAE i               1460
0452    0452    0062        7777                7777
0453    0453    0063        HLT                 0000    ACC error. ACC = 7777; i = 1
0454    0454    0064        LZE i               0472
0455    0455    0065        HLT                 0000    Error. Link bit ≠ 1
0456    0456    0066        CLR                 0011
0457    0457    0067    #5R 0                   0000    ROL i order
0460    0460    0070        SAE i               1460
0461    0461    0071        0                   0000
0462    0462    0072        HLT                 0000    ACC error. ACC = 0; i = 1
0463    0463    0073        LZE                 0452
0464    0464    0074        HLT                 0000    Error. Link bit ≠ 0
0465    0465    0075        LDA i               1020
0466    0466    0076        1                   0001    Increment count bits of ROL orders
0467    0467    0077        ADM                 1140
```

```
0470  0100        2R              0422  [ROLT5
0471  0101        STC 3R          4435
0472  0102        LDA i           1020  Increment count bits of
0473  0103        1               0001  ROL i orders
0474  0104        ADM             1140
0475  0105        4R              0450
0476  0106        STC 5R          4457
0477  0107        XSK i 2         0222
0500  0110        JMP 2B          6417
0501  0111        XSK i 1         0221
0502  0112        JMP 2A          6403
0503  0113        JMP 1T          6034  To next test
```

```
                0001    [RORT1
                0002    [ROR TEST 1
                0003    [FLOAT 1
                0004    [i=0
                0005    ⊟400
0400            0006        12                  0012    Test number
0401            0007    #2S SET i 1             0061    Do test 10 times
0402            0010        7767                7767
0403            0011    #2A SET i 3             0063    Do 14 patterns
0404            0012        7763                7763
0405            0013        SET i 4             0064    Set test constant address
0406            0014        2T-1 .              0447
0407            0015    #2B SET i 5             0065    Shift count
0410            0016        0                   0000
0411            0017        SET i 6             0066    Do 20 counts, 0 - 17
0412            0020        7757                7757
0413            0021        XSK i 4             0224    Increment test constant address
0414            0022    #2C LDA                 1000
0415            0023        2R                  0433
0416            0024        BCL i               1560
0417            0025        17                  0017    Clear count bits
0420            0026        STC 2R              4433
0421            0027        LDA                 1000
0422            0030        2R                  0433
0423            0031        BSE                 1600    Set shift count
0424            0032        5                   0005
0425            0033        STC 2R              4433
0426            0034        ADD 4               2004
0427            0035        ADD 5               2005    Compute address of test result
0430            0036        STC 7               4007
0431            0037        CLR                 0011    Clear link bit
0432            0040        LDA 4               1004
0433            0041    #2R ROR                 0300
0434            0042        SAE 7               1447
0435            0043        HLT                 0000    ACC error
0436            0044        LZE                 0452
0437            0045        HLT                 0000    Error. Link bit ≠ 0
0440            0046        XSK i 5             0225
0441            0047        XSK i 6             0226
0442            0050        JMP 2C              6414
0443            0051        XSK i 3             0223
0444            0052        JMP 2B              6407
0445            0053        XSK i 1             0221
0446            0054        JMP 2A              6403
0447            0055        JMP 1T              6034    To next test
0450            0056    #2T 4000                4000
0451            0057        2000                2000
0452            0060        1000                1000
0453            0061        400                 0400
0454            0062        200                 0200
0455            0063        100                 0100
0456            0064        40                  0040    Float 1
0457            0065        20                  0020
0460            0066        10                  0010
0461            0067        4                   0004
0462            0070        2                   0002
0463            0071        1                   0001
0464            0072        4000                4000
0465            0073        2000                2000
0466            0074        1000                1000
0467            0075        400                 0400
0470            0076        200                 0200
0471            0077        100                 0100
```

0472	0100	40	0040	[RORT1
0473	0101	20	0020	
0474	0102	10	0010	
0475	0103	4	0004	Float 1
0476	0104	2	0002	
0477	0105	1	0001	
0500	0106	4000	4000	
0501	0107	2000	2000	
0502	0110	1000	1000	
0503	0111	400	0400	

```
                0001    [ROR TEST 2
                0002    [FLOAT 0
                0003    [i=0
                0004    ■400
0400            0005        13                  0013    Test number
0401            0006    #2S SET i 1             0061    Do test 10 times
0402            0007        7767                7767
0403            0010    #2A SET i 3             0063    Do 14 patterns
0404            0011        7763                7763
0405            0012        SET i 4             0064    Set test constant address
0406            0013        2T-1                0451
0407            0014    #2B SET i 5             0065    Shift count
0410            0015        0                   0000
0411            0016        SET i 6             0066    Do 20 counts, 0 - 17
0412            0017        7757                7757
0413            0020        XSK i 4             0224    Increment test constant address
0414            0021    #2C LDA                 1000
0415            0022        2R                  0435
0416            0023        BCL i               1560    Clear count bits
0417            0024        17                  0017
0420            0025        STC 2R              4435
0421            0026        LDA                 1000
0422            0027        2R                  0435
0423            0030        BSE                 1600    Set shift count → ROR
0424            0031        5                   0005
0425            0032        STC 2R              4435
0426            0033        ADD 4               2004
0427            0034        ADD 5               2005    Compute address of test result
0430            0035        STC 7               4007
0431            0036        LDA i               1020
0432            0037        4000                4000    Set link bit
0433            0040        ROL i 1             0261
0434            0041        LDA 4               1004
0435            0042    #2R ROR                 0300
0436            0043        SAE 7               1447
0437            0044        HLT                 0000    ACC error
0440            0045        LZE i               0472
0441            0046        HLT                 0000    Error. Link bit ≠ 1
0442            0047        XSK i 5             0225
0443            0050        XSK i 6             0226
0444            0051        JMP 2C              6414
0445            0052        XSK i 3             0223
0446            0053        JMP 2B              6407
0447            0054        XSK i 1             0221
0450            0055        JMP 2A              6403
0451            0056        JMP 1T              6034    Next test
0452            0057    #2T 3777                3777
0453            0060        5777                5777
0454            0061        6777                6777
0455            0062        7377                7377
0456            0063        7577                7577
0457            0064        7677                7677
0460            0065        7737                7737
0461            0066        7757                7757
0462            0067        7767                7767
0463            0070        7773                7773
0464            0071        7775                7775
0465            0072        7776                7776
0466            0073        3777                3777
0467            0074        5777                5777
0470            0075        6777                6777
0471            0076        7377                7377
```

```
0472    0100    7577    7577    [RORT2
0473    0101    7677    7677
0474    0102    7737    7737
0475    0103    7757    7757
0476    0104    7767    7767
0477    0105    7773    7773
0500    0106    7775    7775
0501    0107    7776    7776
0502    0110    3777    3777
0503    0111    5777    5777
0504    0112    6777    6777
0505    0113    7377    7377
```

```
                0001    [RORT3
                0002    [ROR TEST 3
                0003    [FLOAT 1
                0004    [i=1
                0005    ⊟400
0400            0006        14                  0014  Test number
0401            0007    #2S SET i 1             0061  Do test 10 times
0402            0010        7767                7767
0403            0011    #2A SET i 3             0063  Do 14 patterns
0404            0012        7763                7763
0405            0013        SET i 4             0064  Set test constant address
0406            0014        2T-1                0445
0407            0015    #2B SET i 5             0065  Shift couner
0410            0016        0                   0000
0411            0017        SET i 6             0066  Do 20 counts, 0 - 17
0412            0020        7757                7757
0413            0021        XSK i 4             0224  Increment test constant address
0414            0022    #2C LDA                 1000
0415            0023        2R                  0433
0416            0024        BCL i               1560
0417            0025        17                  0017  Clear count bits in ROR
0420            0026        STC 2R              4433
0421            0027        LDA                 1000
0422            0030        2R                  0433
0423            0031        BSE                 1600  Set shift count → ROR
0424            0032        5                   0005
0425            0033        STC 2R              4433
0426            0034        ADD 4               2004
0427            0035        ADD 5               2005  Compute address of test result
0430            0036        STC 7               4007
0431            0037        CLR                 0011
0432            0040        LDA 4               1004
0433            0041    #2R ROR i               0320
0434            0042        SAE 7               1447
0435            0043        HLT                 0000  Error in ACC
0436            0044        XSK i 5             0225  Increment shift count
0437            0045        XSK i 6             0226
0440            0046        JMP 2C              6414
0441            0047        XSK i 3             0223
0442            0050        JMP 2B              6407
0443            0051        XSK i 1             0221
0444            0052        JMP 2A              6403
0445            0053        JMP 1T              6034  Next test
0446            0054    #2T 4000                4000
0447            0055        2000                2000
0450            0056        1000                1000
0451            0057        400                 0400
0452            0060        200                 0200
0453            0061        100                 0100
0454            0062        40                  0040
0455            0063        20                  0020
0456            0064        10                  0010
0457            0065        4                   0004
0460            0066        2                   0002
0461            0067        1                   0001
0462            0070        0                   0000
0463            0071        4000                4000
0464            0072        2000                2000
0465            0073        1000                1000
0466            0074        400                 0400
0467            0075        200                 0200
0470            0076        100                 0100
0471            0077        40                  0040
```

```
0472    0100    20          0020    [RORT3
0473    0101    10          0010
0474    0102    4           0004
0475    0103    2           0002
0476    0104    1           0001
0477    0105    0           0000
0500    0106    4000        4000
0501    0107    2000        2000
0502    0110    1000        1000
```

```
                0001    [RORT4
                0002    [ROR TEST 4
                0003    [FLOAT 0
                0004    [i=1
                0005    ⊟400
0400            0006        15                  0016  Test number
0401            0007    #2S SET i 1             0061  Do test 10 times
0402            0010        7767                7767
0403            0011    #2A SET i 3             1020  Do 14 patterns
0404            0012        7763                0300
0405            0013        SET i 4             1040  Set test constant address
0406            0014        2T-1                0422
0407            0015    #2B SET i 5             4435  Shift count
0410            0016        0                   1020
0411            0017        SET i 6             0320  Do 20 counts, 0 - 17
0412            0020        7757                1040
0413            0021        XSK i 4             0450  Increment test constant address
0414            0022    #2C LDA                 4457
0415            0023        2R                  0062
0416            0024        BCL i               7757  Clear count bits in ROR
0417            0025        17                  0011
0420            0026        STC 2R              1020
0421            0027        LDA                 7777
0422            0030        2R                  0000
0423            0031        BSE                 1460  Set shift count → ROR
0424            0032        5                   7777
0425            0033        STC 2R              0000
0426            0034        ADD 4               0452
0427            0035        ADD 5               0000  Compute address of test result
0430            0036        STC 7               1020
0431            0037        LDA i               4000
0432            0040        4000                0261  Set link bit
0433            0041        ROL i 1             1020
0434            0042        LDA 4               0000
0435            0043    #2R ROR i               0000
0436            0044        SAE 7               1460
0437            0045        HLT                 0000  Error
0440            0046        XSK i 5             0000  Increment shift count
0441            0047        XSK i 6             0472
0442            0050        JMP 2C              0000
0443            0051        XSK i 3             1020
0444            0052        JMP 2B              4000
0445            0053        XSK i 1             0261
0446            0054        JMP 2A              1020
0447            0055        JMP 1T              7777  To next test
0450            0056    #2T 3777                0000
0451            0057        5777                1460
0452            0060        6777                7777
0453            0061        7377                0000
0454            0062        7577                0472
0455            0063        7677                0000
0456            0064        7737                0011
0457            0065        7757                0000
0460            0066        7767                1460
0461            0067        7773                0000
0462            0070        7775                0000
0463            0071        7776                0452
0464            0072        7777                0000
0465            0073        3777                1020
0466            0074        5777                0001
0467            0075        6777                1140
0470            0076        7377                0422
0471            0077        7577                4435
```

```
0472    0100    7677    1020    [RORT4
0473    0101    7737    0001
0474    0102    7757    1140
0475    0103    7767    0450
0476    0104    7773    4457
0477    0105    7775    0222
0500    0106    7776    6417
0501    0107    7777    0221
0502    0110    3777    6403
0503    0111    5777    6034
0504    0112    6777    0000
```

```
                0001    [RORT5
                0002    [ROR TEST 5
                0003    [ALL 1 OR
                0004    [ALL 0
                0005    [i=0 OR
                0006    [i=1
                0007    ⊟400
0400            0010        16              0016  Test number
0401            0011    #2S SET i 1         0061  Do test 10 times
0402            0012        7767            7767
0403            0013    #2A LDA i           1020
0404            0014        ROR             0300
0405            0015        STA             1040  Set up 2 ROR orders
0406            0016        2R              0422
0407            0017        STC 3R          4435
0410            0020        LDA i           1020
0411            0021        ROR i           0320
0412            0022        STA             1040
0413            0023        4R              0450  Set up 2 ROR i orders
0414            0024        STC 5R          4457
0415            0025        SET i 2         0062  Do 20 counts, 0 - 17
0416            0026        7757            7757
0417            0027    [#2B CLR            0011
0420            0030        LDA i           1020
0421            0031        7777            7777
0422            0032    [#2R 0              0000  ROR
0423            0033        SAE i           1460
0424            0034        7777            7777
0425            0035        HLT             0000  ACC error. ACC = 7777; i = 0
0426            0036        LZE             0452
0427            0037        HLT             0000  Error. Link bit ≠ 0
0430            0040    [   LDA i           1020
0431            0041    |   4000            4000  Set link bit
0432            0042    |   ROL i 1         0261
0433            0043    |   LDA i           1020
0434            0044    |   0               0000  ROR
0435            0045    [#3R 0              0000
0436            0046        SAE i           1460
0437            0047        0               0000
0440            0050        HLT             0000  ACC error. ACC = 0; i = 0
0441            0051        LZE i           0472
0442            0052        HLT             0000  Error. Link bit ≠ 1
0443            0053    [   LDA i           1020
0444            0054    |   4000            4000
0445            0055    |   ROL i 1         0261  Set link bit
0446            0056    |   LDA i           1020
0447            0057    |   7777            7777
0450            0060    [#4R 0              0000  ROR i
0451            0061        SAE i           1460
0452            0062        7777            7777
0453            0063        HLT             0000  ACC error. ACC = 7777; i = 1
0454            0064        LZE i           0472
0455            0065        HLT             0000  Error. Link bit ≠ 1
0456            0066    [   CLR             0011
0457            0067    [#5R 0              0000  ROR i
0460            0070        SAE i           1460
0461            0071        0               0000
0462            0072        HLT             0000  ACC error. ACC = 0; i = 1
0463            0073        LZE             0452
0464            0074        HLT             0000  Error. Link bit ≠ 0
0465            0075        LDA i           1020
0466            0076        1               0001  Increment count in ROR orders
0467            0077        ADM             1140
```

```
0470    0100    2R          0422    [RORT5
0471    0101    STC 3R      4435
0472    0102    LDA i       1020
0473    0103    1           0001
0474    0104    ADM         1140    Increment count in ROR i orders
0475    0105    4R          0450
0476    0106    STC 5R      4457
0477    0107    XSK i 2     0222
0500    0110    JMP 2B      6417
0501    0111    XSK i 1     0221
0502    0112    JMP 2A      6403
0503    0113    JMP 1T      6034    To next test
```

```
         0001     [CLRTST
         0002     [CLR TEST
         0003     @400
0400     0004          17              0017 Test number
0401     0005     #2S  SET i 1         0061 Do test 10 times
0402     0006          7767            7767
0403     0007     #2A  LDA i           1020
0404     0010          4000            4000
0405     0011          ROL i 1         0261 Set link bit
0406     0012          LDA i           1020
0407     0013          7777            7777
0410     0014          CLR             0011
0411     0015          SAE i           1460
0412     0016          0               0000 ACC error
0413     0017          HLT             0000
0414     0020          LZE             0452
0415     0021          HLT             0000 Error. Link bit ≠ 0
0416     0022          XSK i 1         0221
0417     0023          JMP 2A          6403
0420     0024          JMP 1T          6034 To next test
```

```
                0001    [ADDONE
                0002    [ADD ONE TEST
                0003    ⊟400
0400            0004        20              0020  Test number
0401            0005    #2S SET i 1         0061  Do test 10 times
0402            0006        7767            7767
0403            0007    #2A CLR             0011  Set check counter = 0
0404            0010        STC 2B+1        4411
0405            0011        SET i 4         0064  Do outer loop 4 times
0406            0012        7773            7773
0407            0013        CLR             0011
0410            0014    #2B SET i 2         0062  Set check counter
0411            0015        0               0000
0412            0016        SET i 3         0063  Do inner loop 1777 times
0413            0017        0               0000
0414            0020    [#3A ADA i          1120  Increment ACC
0415            0021    [   1               0001
0416            0022        XSK i 2         0222  Increment check counter
0417            0023        NOP             0016
0420            0024        SAE             1440
0421            0025        2               0002
0422            0026        HLT             0000  Error
0423            0027        XSK i 3         0223  Do inner loop
0424            0030        JMP 3A          6414
0425            0031        ADA i           1120  Fix ACC count for next loop
0426            0032        1               0001
0427            0033        LDA i           1020
0430            0034        2000            2000
0431            0035        ADM             1140  Increment bits 11, 10 of
0432            0036        2B+1            0411  check counter
0433            0037        XSK i 4         0224
0434            0040        JMP 2B          6410
0435            0041        XSK i 1         0221
0436            0042        JMP 2A          6403
0437            0043        JMP 1T          6034  To next test
```

```
                0001    [COMT1
                0002    [COM TEST 1
                0003    ⊟400
0400            0004        21              0021    Test number
0401            0005    #2S SET i 1         0061    Do test 10 times
0402            0006        7767            7767
0403            0007    #2A LDA i           1020
0404            0010        2T              0436    Initial test constant address
0405            0011        STC 2L+1        4414
0406            0012        LDA i           1020
0407            0013        3T              0472    Initial result address
0410            0014        STC 2C+1        4417
0411            0015        SET i 2         0062    Loop thru patterns
0412            0016        JMP 2T-3T-1     7742
0413            0017    #2L LDA             1000
0414            0020        0               0000
0415            0021        COM             0017
0416            0022    #2C SAE             1440
0417            0023        0               0000
0420            0024        HLT             0000    Error.
0421            0025        LDA i           1020
0422            0026        1               0001
0423            0027        ADM             1140    Increment test constant address
0424            0030        2L+1            0414
0425            0031        LDA i           1020
0426            0032        1               0001
0427            0033        ADM             1140    Increment test result address
0430            0034        2C+1            0417
0431            0035        XSK i 2         0222
0432            0036        JMP 2L          6413
0433            0037        XSK i 1         0221
0434            0040        JMP 2A          6403
0435            0041        JMP 1T          6034
0436            0042    #2T 0               0000
0437            0043        7777            7777
0440            0044        5252            5252
0441            0045        2525            2525
0442            0046        1               0001
0443            0047        2               0002
0444            0050        4               0004
0445            0051        10              0010
0446            0052        20              0020
0447            0053        40              0040
0450            0054        100             0100
0451            0055        200             0200
0452            0056        400             0400
0453            0057        1000            1000    Test constants
0454            0060        2000            2000
0455            0061        4000            4000
0456            0062        7776            7776
0457            0063        7775            7775
0460            0064        7773            7773
0461            0065        7767            7767
0462            0066        7757            7757
0463            0067        7737            7737
0464            0070        7677            7677
0465            0071        7577            7577
0466            0072        7377            7377
0467            0073        6777            6777
0470            0074        5777            5777
0471            0075        3777            3777
0472            0076    #3T 7777            7777
0473            0077        0               0000
```

0474	0100	2525	2525	[COMT]
0475	0101	5252	5252	
0476	0102	7776	7776	
0477	0103	7775	7775	
0500	0104	7773	7773	
0501	0105	7767	7767	
0502	0106	7757	7757	
0503	0107	7737	7737	
0504	0110	7677	7677	
0505	0111	7577	7577	
0506	0112	7377	7377	
0507	0113	6777	6777	
0510	0114	5777	5777	Test results
0511	0115	3777	3777	
0512	0116	1	0001	
0513	0117	2	0002	
0514	0120	4	0004	
0515	0121	10	0010	
0516	0122	20	0020	
0517	0123	40	0040	
0520	0124	100	0100	
0521	0125	200	0200	
0522	0126	400	0400	
0523	0127	1000	1000	
0524	0130	2000	2000	
0525	0131	4000	4000	

```
                0001    [SCRT1
                0002    [SCR TEST 1
                0003    [FLOAT 1
                0004    [i=0
                0005    @400
0400            0006        22                  0022  Test number
0401            0007    #2S SET i 1             0061  Do test 10 times
0402            0010        7767                7767
0403            0011    #2A SET i 2             0062  Do 14 patterns
0404            0012        7763                7763
0405            0013        SET i 3             0063  Set initial test constant address
0406            0014        2T                  0444
0407            0015        SET i 4             0064  Set initial test result address
0410            0016        2T-1                0443
0411            0017    #2B LDA i               1020
0412            0020        SCR                 0340
0413            0021        STC 2X              4420  Clear count bits
0414            0022        SET i 5             0065  Do 20 counts, 0 - 17
0415            0023        7757                7757
0416            0024    [#2C CLR                0011  Clear link bit
0417            0025        LDA 3               1003
0420            0026    [#2X 0                  0000  SCR order
0421            0027        SAE i 4             1464
0422            0030        HLT                 0000  ACC error
0423            0031        LZE                 0452
0424            0032        HLT                 0000  Error. Link bit ≠ 0
0425            0033        LDA i               1020
0426            0034        1                   0001
0427            0035        ADM                 1140  Increment shift count
0430            0036        2X                  0420
0431            0037        XSK i 5             0225
0432            0040        JMP 2C              6416  Do 20 counts
0433            0041        LDA i               1020
0434            0042        20                  0020
0435            0043        ADM                 1140  Increment test constant address
0436            0044        3                   0003
0437            0045        XSK i 2             0222
0440            0046        JMP 2B              6411  Do 14 patterns
0441            0047        XSK i 1             0221
0442            0050        JMP 2A              6403
0443            0051        JMP 1T              6034
0444            0052    #2T 4000                4000
0445            0053        6000                6000
0446            0054        7000                7000  Test constants and test results
0447            0055        7400                7400
0450            0056        7600                7600
0451            0057        7700                7700
0452            0060        7740                7740
0453            0061        7760                7760
0454            0062        7770                7770
0455            0063        7774                7774
0456            0064        7776                7776
0457            0065        7777                7777
0460            0066        7777                7777
0461            0067        7777                7777
0462            0070        7777                7777
0463            0071        7777                7777
0464            0072        2000                2000
0465            0073        1000                1000
0466            0074        400                 0400
0467            0075        200                 0200
0470            0076        100                 0100
0471            0077        40                  0040
```

Test constants and test results

0472	0100	20	0020
0473	0101	10	0010
0474	0102	4	0004
0475	0103	2	0002
0476	0104	1	0001
0477	0105	0	0000
0500	0106	0	0000
0501	0107	0	0000
0502	0110	0	0000
0503	0111	0	0000
0504	0112	1000	1000
0505	0113	400	0400
0506	0114	200	0200
0507	0115	100	0100
0510	0116	40	0040
0511	0117	20	0020
0512	0120	10	0010
0513	0121	4	0004
0514	0122	2	0002
0515	0123	1	0001
0516	0124	0	0000
0517	0125	0	0000
0520	0126	0	0000
0521	0127	0	0000
0522	0130	0	0000
0523	0131	0	0000
0524	0132	400	0400
0525	0133	200	0200
0526	0134	100	0100
0527	0135	40	0040
0530	0136	20	0020
0531	0137	10	0010
0532	0140	4	0004
0533	0141	2	0002
0534	0142	1	0001
0535	0143	0	0000
0536	0144	0	0000
0537	0145	0	0000
0540	0146	0	0000
0541	0147	0	0000
0542	0150	0	0000
0543	0151	0	0000
0544	0152	200	0200
0545	0153	100	0100
0546	0154	40	0040
0547	0155	20	0020
0550	0156	10	0010
0551	0157	4	0004
0552	0160	2	0002
0553	0161	1	0001
0554	0162	0	0000
0555	0163	0	0000
0556	0164	0	0000
0557	0165	0	0000
0560	0166	0	0000
0561	0167	0	0000
0562	0170	0	0000
0563	0171	0	0000
0564	0172	100	0100
0565	0173	40	0040
0566	0174	20	0020
0567	0175	10	0010
0570	0176	4	0004
0571	0177	2	0002

0572	0200	1	0001
0573	0201	0	0000
0574	0202	0	0000
0575	0203	0	0000
0576	0204	0	0000
0577	0205	0	0000
0600	0206	0	0000
0601	0207	0	0000
0602	0210	0	0000
0603	0211	0	0000
0604	0212	40	0040
0605	0213	20	0020
0606	0214	10	0010
0607	0215	4	0004
0610	0216	2	0002
0611	0217	1	0001
0612	0220	0	0000
0613	0221	0	0000
0614	0222	0	0000
0615	0223	0	0000
0616	0224	0	0000
0617	0225	0	0000
0620	0226	0	0000
0621	0227	0	0000
0622	0230	0	0000
0623	0231	0	0000
0624	0232	20	0020
0625	0233	10	0010
0626	0234	4	0004
0627	0235	2	0002
0630	0236	1	0001
0631	0237	0	0000
0632	0240	0	0000
0633	0241	0	0000
0634	0242	0	0000
0635	0243	0	0000
0636	0244	0	0000
0637	0245	0	0000
0640	0246	0	0000
0641	0247	0	0000
0642	0250	0	0000
0643	0251	0	0000
0644	0252	10	0010
0645	0253	4	0004
0646	0254	2	0002
0647	0255	1	0001
0650	0256	0	0000
0651	0257	0	0000
0652	0260	0	0000
0653	0261	0	0000
0654	0262	0	0000
0655	0263	0	0000
0656	0264	0	0000
0657	0265	0	0000
0660	0266	0	0000
0661	0267	0	0000
0662	0270	0	0000
0663	0271	0	0000
0664	0272	4	0004
0665	0273	2	0002
0666	0274	1	0001
0667	0275	0	0000
0670	0276	0	0000
0671	0277	0	0000

0672	0300	0	0000
0673	0301	0	0000
0674	0302	0	0000
0675	0303	0	0000
0676	0304	0	0000
0677	0305	0	0000
0700	0306	0	0000
0701	0307	0	0000
0702	0310	0	0000
0703	0311	0	0000
0704	0312	2	0002
0705	0313	1	0001
0706	0314	0	0000
0707	0315	0	0000
0710	0316	0	0000
0711	0317	0	0000
0712	0320	0	0000
0713	0321	0	0000
0714	0322	0	0000
0715	0323	0	0000
0716	0324	0	0000
0717	0325	0	0000
0720	0326	0	0000
0721	0327	0	0000
0722	0330	0	0000
0723	0331	0	0000
0724	0332	1	0001
0725	0333	0	0000
0726	0334	0	0000
0727	0335	0	0000
0730	0336	0	0000
0731	0337	0	0000
0732	0340	0	0000
0733	0341	0	0000
0734	0342	0	0000
0735	0343	0	0000
0736	0344	0	0000
0737	0345	0	0000
0740	0346	0	0000
0741	0347	0	0000
0742	0350	0	0000
0743	0351	0	0000

```
                0001    [SCRT2
                0002    [SCR TEST 2
                0003    [FLOAT 0
                0004    [i=0
                0005    @400
0400            0006        23                  7676  Test number
0401            0007    #2S SET i 1             7676  Do test 10 times
0402            0010        7767                0112
0403            0011    #2A SET i 2             3336  Do 14 patterns
0404            0012        7763                5706
0405            0013        SET i 3             0000  Set initial test constant address
0406            0014        2T                  1410
0407            0015        SET i 4             1431  Set initial test result address
0410            0016        2T-1                0111
0411            0017    #2B LDA i               0000
0412            0020        SCR                 0000  Clear count bits
0413            0021        STC 2X              0000
0414            0022        SET i 5             0000  Do 20 counts, 0 - 17
0415            0023        7757                0000
0416            0024    [#2C LDA i              0000
0417            0025    |   4000                0000  Set link bit
0420            0026    |   ROL i 1             0000
0421            0027    |   LDA 3               0000
0422            0030    [#2X 0                  0000  SCR order
0423            0031        SAE i 4             0000
0424            0032        HLT                 0000  ACC error
0425            0033        LZE i               0000
0426            0034        HLT                 0000  Error. Link bit ≠ 1
0427            0035        LDA i               0000
0430            0036        1                   0000
0431            0037        ADM                 0000  Increment shift count
0432            0040        2X                  0000
0433            0041        XSK i 5             0000
0434            0042        JMP 2C              0000  Do 20 counts
0435            0043        LDA i               0000
0436            0044        20                  0000
0437            0045        ADM                 0000  Increment test constant address
0440            0046        3                   0000
0441            0047        XSK i 2             0000
0442            0050        JMP 2B              0000  Do 14 patterns
0443            0051        XSK i 1             0000
0444            0052        JMP 2A              0000
0445            0053        JMP 1T              0000
0446            0054    #2T 3777                0000
0447            0055        1777                0000
0450            0056        777                 0000  Test constants and test results
0451            0057        377                 0000
0452            0060        177                 0000
0453            0061        77                  0000
0454            0062        37                  0000
0455            0063        17                  0000
0456            0064        7                   0000
0457            0065        3                   0000
0460            0066        1                   0000
0461            0067        0                   0000
0462            0070        0                   0000
0463            0071        0                   0000
0464            0072        0                   0000
0465            0073        0                   0000
0466            0074        5777                0000
0467            0075        6777                0000
0470            0076        7377                0000
0471            0077        7577                0000
```

Test constants and test results

0472	0100	7677	0000
0473	0101	7737	0000
0474	0102	7757	0000
0475	0103	7767	0000
0476	0104	7773	0000
0477	0105	7775	0000
0500	0106	7776	0000
0501	0107	7777	0000
0502	0110	7777	0000
0503	0111	7777	0000
0504	0112	7777	0000
0505	0113	7777	0000
0506	0114	6777	0000
0507	0115	7377	0000
0510	0116	7577	0000
0511	0117	7677	0000
0512	0120	7737	0000
0513	0121	7757	0000
0514	0122	7767	0000
0515	0123	7773	0000
0516	0124	7775	0000
0517	0125	7776	0000
0520	0126	7777	0000
0521	0127	7777	0000
0522	0130	7777	0000
0523	0131	7777	0000
0524	0132	7777	0000
0525	0133	7777	0000
0526	0134	7377	0000
0527	0135	7577	0000
0530	0136	7677	0000
0531	0137	7737	0000
0532	0140	7757	0000
0533	0141	7767	0000
0534	0142	7773	0000
0535	0143	7775	0000
0536	0144	7776	0000
0537	0145	7777	0000
0540	0146	7777	0000
0541	0147	7777	0000
0542	0150	7777	0000
0543	0151	7777	0000
0544	0152	7777	0000
0545	0153	7777	0000
0546	0154	7577	0000
0547	0155	7677	0000
0550	0156	7737	0000
0551	0157	7757	0000
0552	0160	7767	0000
0553	0161	7773	0000
0554	0162	7775	0000
0555	0163	7776	0000
0556	0164	7777	0000
0557	0165	7777	0000
0560	0166	7777	0000
0561	0167	7777	0000
0562	0170	7777	0000
0563	0171	7777	0000
0564	0172	7777	0000
0565	0173	7777	0000
0566	0174	7677	0000
0567	0175	7737	0000
0570	0176	7757	0000
0571	0177	7767	0000

0572	0200	7773	0000
0573	0201	7775	0000
0574	0202	7776	0000
0575	0203	7777	0000
0576	0204	7777	0000
0577	0205	7777	0000
0600	0206	7777	0000
0601	0207	7777	0000
0602	0210	7777	0000
0603	0211	7777	0000
0604	0212	7777	0000
0605	0213	7777	0000
0606	0214	7737	0000
0607	0215	7757	0000
0610	0216	7767	0000
0611	0217	7773	0000
0612	0220	7775	0000
0613	0221	7776	0000
0614	0222	7777	0000
0615	0223	7777	0000
0616	0224	7777	0000
0617	0225	7777	0000
0620	0226	7777	0000
0621	0227	7777	0000
0622	0230	7777	0000
0623	0231	7777	0000
0624	0232	7777	0000
0625	0233	7777	0000
0626	0234	7757	0000
0627	0235	7767	0000
0630	0236	7773	0000
0631	0237	7775	0000
0632	0240	7776	0000
0633	0241	7777	0000
0634	0242	7777	0000
0635	0243	7777	0000
0636	0244	7777	0000
0637	0245	7777	0000
0640	0246	7777	0000
0641	0247	7777	0000
0642	0250	7777	0000
0643	0251	7777	0000
0644	0252	7777	0000
0645	0253	7777	0000
0646	0254	7767	0000
0647	0255	7773	0000
0650	0256	7775	0000
0651	0257	7776	0000
0652	0260	7777	0000
0653	0261	7777	0000
0654	0262	7777	0000
0655	0263	7777	0000
0656	0264	7777	0000
0657	0265	7777	0000
0660	0266	7777	0000
0661	0267	7777	0000
0662	0270	7777	0000
0663	0271	7777	0000
0664	0272	7777	0000
0665	0273	7777	0000
0666	0274	7773	0000
0667	0275	7775	0000
0670	0276	7776	0000
[illegible]	[illegible]	[illegible]	0000

0672	0300	7777	0000
0673	0301	7777	0000
0674	0302	7777	0000
0675	0303	7777	0000
0676	0304	7777	0000
0677	0305	7777	0000
0700	0306	7777	0000
0701	0307	7777	0000
0702	0310	7777	0000
0703	0311	7777	0000
0704	0312	7777	0000
0705	0313	7777	0000
0706	0314	7775	0000
0707	0315	7776	0000
0710	0316	7777	0000
0711	0317	7777	0000
0712	0320	7777	0000
0713	0321	7777	0000
0714	0322	7777	0000
0715	0323	7777	0000
0716	0324	7777	0000
0717	0325	7777	0000
0720	0326	7777	0000
0721	0327	7777	0000
0722	0330	7777	0000
0723	0331	7777	0000
0724	0332	7777	0000
0725	0333	7777	0000
0726	0334	7776	0000
0727	0335	7777	0000
0730	0336	7777	0000
0731	0337	7777	0000
0732	0340	7777	0000
0733	0341	7777	0000
0734	0342	7777	0000
0735	0343	7777	0000
0736	0344	7777	0000
0737	0345	7777	0000
0740	0346	7777	0000
0741	0347	7777	0000
0742	0350	7777	0000
0743	0351	7777	0000
0744	0352	7777	0000
0745	0353	7777	0000

```
0001  [SCRT3
0002  [SCR TEST 3
0003  [FLOAT 1
0004  [i=1
0005  @400
0400  0006      24                  0024   Test number
0401  0007  #2S  SET i 1             0061   Do test 10 times
0402  0010      7767                7767
0403  0011      LDA                 1000   Compute next BN and QN 2
0404  0012      1R+1                0021
0405  0013      ADA i               1120
0406  0014      1001                1001
0407  0015      STC P+2             4411
0410  0016      RDC                 0700   Read next block → QN 2
0411  0017      0                   0000
0412  0020      LDA i               1020   Add 1 to block increment in control
0413  0021      1                   0001
0414  0022      ADM                 1140
0415  0023      1I                  0046
0416  0024  #2A  SET i 2             0062   Do 14 patterns
0417  0025      7763                7763
0420  0026      SET i 3             0063   Set initial test constant address
0421  0027      2T                  0467
0422  0030      SET i 4             0064   Set initial test result address
0423  0031      2T-1                0466
0424  0032      SET i 6             0066   Set initial link bit result check
0425  0033      3T-1                0777
0426  0034  #2B  LDA i              1020   Clear count bits
0427  0035      SCR i               0360
0430  0036      STC 2X              4443
0431  0037      SET i 5             0065   Do 20 counts, 0 - 17
0432  0040      7757                7757
0433  0041  #2C  LDA i              1020   Set up proper LZE order to check link bit results
0434  0042      LZE                 0452
0435  0043      BSE i 6             1626
0436  0044      STC 2L              4446
0437  0045      LDA i               1020   Set link bit
0440  0046      4000                4000
0441  0047      ROL i 1             0261
0442  0050      LDA 3               1003   SCR i order
0443  0051  #2X  0                  0000
0444  0052      SAE i 4             1464   ACC error
0445  0053      HLT                 0000
0446  0054  #2L  0                  0000   LZE or LZE i order
0447  0055      HLT                 0000   Error. Link bit
0450  0056      LDA i               1020   Increment shift count
0451  0057      1                   0001
0452  0060      ADM                 1140
0453  0061      2X                  0443
0454  0062      XSK i 5             0225   Do 20 counts
0455  0063      JMP 2C              6433
0456  0064      LDA i               1020   Increment test constant address
0457  0065      20                  0020
0460  0066      ADM                 1140
0461  0067      3                   0003
0462  0070      XSK i 2             0222   Do 14 patterns
0463  0071      JMP 2B              6426
0464  0072      XSK i 1             0221
0465  0073      JMP 2A              6416
0466  0074      JMP 1T              6034
0467  0075  #2T  4000               4000   Test constants and test results
0470  0076      6000                6000
0471  0077      7000                7000
```

0472	0100	7400	7400
0473	0101	7600	7600
0474	0102	7700	7700
0475	0103	7740	7740
0476	0104	7760	7760
0477	0105	7770	7770
0500	0106	7774	7774
0501	0107	7776	7776
0502	0110	7777	7777
0503	0111	7777	7777
0504	0112	7777	7777
0505	0113	7777	7777
0506	0114	7777	7777
0507	0115	2000	2000
0510	0116	1000	1000
0511	0117	400	0400
0512	0120	200	0200
0513	0121	100	0100
0514	0122	40	0040
0515	0123	20	0020
0516	0124	10	0010
0517	0125	4	0004
0520	0126	2	0002
0521	0127	1	0001
0522	0130	0	0000
0523	0131	0	0000
0524	0132	0	0000
0525	0133	0	0000
0526	0134	0	0000
0527	0135	1000	1000
0530	0136	400	0400
0531	0137	200	0200
0532	0140	100	0100
0533	0141	40	0040
0534	0142	20	0020
0535	0143	10	0010
0536	0144	4	0004
0537	0145	2	0002
0540	0146	1	0001
0541	0147	0	0000
0542	0150	0	0000
0543	0151	0	0000
0544	0152	0	0000
0545	0153	0	0000
0546	0154	0	0000
0547	0155	400	0400
0550	0156	200	0200
0551	0157	100	0100
0552	0160	40	0040
0553	0161	20	0020
0554	0162	10	0010
0555	0163	4	0004
0556	0164	2	0002
0557	0165	1	0001
0560	0166	0	0000
0561	0167	0	0000
0562	0170	0	0000
0563	0171	0	0000
0564	0172	0	0000
0565	0173	0	0000
0566	0174	0	0000
0567	0175	200	0200
0570	0176	100	0100
0571	0177	40	0040

Test constants and test results

0572	0200	20	0020
0573	0201	10	0010
0574	0202	4	0004
0575	0203	2	0002
0576	0204	1	0001
0577	0205	0	0000
0600	0206	0	0000
0601	0207	0	0000
0602	0210	0	0000
0603	0211	0	0000
0604	0212	0	0000
0605	0213	0	0000
0606	0214	0	0000
0607	0215	100	0100
0610	0216	40	0040
0611	0217	20	0020
0612	0220	10	0010
0613	0221	4	0004
0614	0222	2	0002
0615	0223	1	0001
0616	0224	0	0000
0617	0225	0	0000
0620	0226	0	0000
0621	0227	0	0000
0622	0230	0	0000
0623	0231	0	0000
0624	0232	0	0000
0625	0233	0	0000
0626	0234	0	0000
0627	0235	40	0040
0630	0236	20	0020
0631	0237	10	0010
0632	0240	4	0004
0633	0241	2	0002
0634	0242	1	0001
0635	0243	0	0000
0636	0244	0	0000
0637	0245	0	0000
0640	0246	0	0000
0641	0247	0	0000
0642	0250	0	0000
0643	0251	0	0000
0644	0252	0	0000
0645	0253	0	0000
0646	0254	0	0000
0647	0255	20	0020
0650	0256	10	0010
0651	0257	4	0004
0652	0260	2	0002
0653	0261	1	0001
0654	0262	0	0000
0655	0263	0	0000
0656	0264	0	0000
0657	0265	0	0000
0660	0266	0	0000
0661	0267	0	0000
0662	0270	0	0000
0663	0271	0	0000
0664	0272	0	0000
0665	0273	0	0000
0666	0274	0	0000
0667	0275	10	0010
0670	0276	4	0004
0671	0277	2	0002

```
0672    0300        1
0673    0301        0
0674    0302        0
0675    0303        0
0676    0304        0
0677    0305        0
0700    0306        0
0701    0307        0
0702    0310        0
0703    0311        0
0704    0312        0
0705    0313        0
0706    0314        0
0707    0315        4
0710    0316        2
0711    0317        1
0712    0320        0
0713    0321        0
0714    0322        0
0715    0323        0
0716    0324        0
0717    0325        0
0720    0326        0
0721    0327        0
0722    0330        0
0723    0331        0
0724    0332        0
0725    0333        0
0726    0334        0
0727    0335        2
0730    0336        1
0731    0337        0
0732    0340        0
0733    0341        0
0734    0342        0
0735    0343        0
0736    0344        0
0737    0345        0
0740    0346        0
0741    0347        0
0742    0350        0
0743    0351        0
0744    0352        0
0745    0353        0
0746    0354        0
0747    0355        1
0750    0356        0
0751    0357        0
0752    0360        0
0753    0361        0
0754    0362        0
0755    0363        0
0756    0364        0
0757    0365        0
0760    0366        0
0761    0367        0
0762    0370        0
0763    0371        0
0764    0372        0
0765    0373        0
0766    0374        0
        0375    ⊟1000
1000    0376    #3T i
1001    0377        0  i Bit for LZE order
```

```
1002    0400        0       0000    [SCRT3
1003    0401        0       0000
1004    0402        0       0000    i bit for LZE order
1005    0403        0       0000
1006    0404        0       0000
1007    0405        0       0000
1010    0406        0       0000
1011    0407        0       0000
1012    0410        0       0000
1013    0411        0       0000
1014    0412        i       0020
1015    0413        i       0020
1016    0414        i       0020
1017    0415        i       0020
1020    0416        i       0020
1021    0417        0       0000
1022    0420        0       0000
1023    0421        0       0000
1024    0422        0       0000
1025    0423        0       0000
1026    0424        0       0000
1027    0425        0       0000
1030    0426        0       0000
1031    0427        0       0000
1032    0430        0       0000
1033    0431        i       0020
1034    0432        0       0000
1035    0433        0       0000
1036    0434        0       0000
1037    0435        0       0000
1040    0436        i       0020
1041    0437        0       0000
1042    0440        0       0000
1043    0441        0       0000
1044    0442        0       0000
1045    0443        0       0000
1046    0444        0       0000
1047    0445        0       0000
1050    0446        0       0000
1051    0447        0       0000
1052    0450        i       0020
1053    0451        0       0000
1054    0452        0       0000
1055    0453        0       0000
1056    0454        0       0000
1057    0455        0       0000
1060    0456        i       0020
1061    0457        0       0000
1062    0460        0       0000
1063    0461        0       0000
1064    0462        0       0000
1065    0463        0       0000
1066    0464        0       0000
1067    0465        0       0000
1070    0466        0       0000
1071    0467        i       0020
1072    0470        0       0000
1073    0471        0       0000
1074    0472        0       0000
1075    0473        0       0000
1076    0474        0       0000
1077    0475        0       0000
1100    0476        i       0020
```

```
1102    0500        0       0000    [SCRT3
1103    0501        0       0000
1104    0502        0       0000    i bit for LZE order
1105    0503        0       0000
1106    0504        0       0000
1107    0505        0       0000
1110    0506        i       0020
1111    0507        0       0000
1112    0510        0       0000
1113    0511        0       0000
1114    0512        0       0000
1115    0513        0       0000
1116    0514        0       0000
1117    0515        0       0000
1120    0516        i       0020
1121    0517        0       0000
1122    0520        0       0000
1123    0521        0       0000
1124    0522        0       0000
1125    0523        0       0000
1126    0524        0       0000
1127    0525        i       0020
1130    0526        0       0000
1131    0527        0       0000
1132    0530        0       0000
1133    0531        0       0000
1134    0532        0       0000
1135    0533        0       0000
1136    0534        0       0000
1137    0535        0       0000
1140    0536        i       0020
1141    0537        0       0000
1142    0540        0       0000
1143    0541        0       0000
1144    0542        0       0000
1145    0543        0       0000
1146    0544        i       0020
1147    0545        0       0000
1150    0546        0       0000
1151    0547        0       0000
1152    0550        0       0000
1153    0551        0       0000
1154    0552        0       0000
1155    0553        0       0000
1156    0554        0       0000
1157    0555        0       0000
1160    0556        i       0020
1161    0557        0       0000
1162    0560        0       0000
1163    0561        0       0000
1164    0562        0       0000
1165    0563        i       0020
1166    0564        0       0000
1167    0565        0       0000
1170    0566        0       0000
1171    0567        0       0000
1172    0570        0       0000
1173    0571        0       0000
1174    0572        0       0000
1175    0573        0       0000
1176    0574        0       0000
1177    0575        0       0000
1200    0576        i       0020
1201    0577        0       0000
```

```
1202    0600        0       0000    [SCRT3
1203    0601        0       0000
1204    0602        i       0020    i bit for LZE order
1205    0603        0       0000
1206    0604        0       0000
1207    0605        0       0000
1210    0606        0       0000
1211    0607        0       0000
1212    0610        0       0000
1213    0611        0       0000
1214    0612        0       0000
1215    0613        0       0000
1216    0614        0       0000
1217    0615        0       0000
1220    0616        i       0020
1221    0617        0       0000
1222    0620        0       0000
1223    0621        i       0020
1224    0622        0       0000
1225    0623        0       0000
1226    0624        0       0000
1227    0625        0       0000
1230    0626        0       0000
1231    0627        0       0000
1232    0630        0       0000
1233    0631        0       0000
1234    0632        0       0000
1235    0633        0       0000
1236    0634        0       0000
1237    0635        0       0000
1240    0636        i       0020
1241    0637        0       0000
1242    0640        i       0020
1243    0641        0       0000
1244    0642        0       0000
1245    0643        0       0000
1246    0644        0       0000
1247    0645        0       0000
1250    0646        0       0000
1251    0647        0       0000
1252    0650        0       0000
1253    0651        0       0000
1254    0652        0       0000
1255    0653        0       0000
1256    0654        0       0000
1257    0655        0       0000
1260    0656        i       0020
1261    0657        i       0020
1262    0660        0       0000
1263    0661        0       0000
1264    0662        0       0000
1265    0663        0       0000
1266    0664        0       0000
1267    0665        0       0000
1270    0666        0       0000
1271    0667        0       0000
1272    0670        0       0000
1273    0671        0       0000
1274    0672        0       0000
1275    0673        0       0000
1276    0674        0       0000
1277    0675        0       0000
```

```
                0001    [SCRT4
                0002    [SCR TEST 4
                0003    [FLOAT 0
                0004    [i=1
                0005    ⊟400
0400            0006        25                  0025    Test number
0401            0007    #2S SET i 1             0061 ]  Do test 10 times
0402            0010        7767                7767 ]
0403            0011        LDA                 1000 ]
0404            0012        1R+1                0021 |
0405            0013        ADA i               1120 |  Compute next BN and QN 2
0406            0014        1001                1001 |
0407            0015        STC ⊅+2             4411 ]
0410            0016        RDC                 0700 ]
0411            0017        0                   0000 ]  Read next block → QN 2
0412            0020        LDA i               1020 ]
0413            0021        1                   0001 |
0414            0022        ADM                 1140 |  Add 1 to block increment in contrl
0415            0023        1I                  0046 ]
0416            0024    #2A SET i 2             0062 ]  Do 14 patterns
0417            0025        7763                7763 ]
0420            0026        SET i 3             0063 ]  Set initial test constant address
0421            0027        2T                  0465 ]
0422            0030        SET i 4             0064 ]  Set initial test result address
0423            0031        2T-1                0464 ]
0424            0032        SET i 6             0066 ]  Set initial link bit result check
0425            0033        3T-1                0777 ]
0426            0034    #2B LDA i               1020 ]
0427            0035        SCR i               0360 |  Clear count bits
0430            0036        STC 2X              4441 ]
0431            0037        SET i 5             0065 ]  Do 20 counts, 0 - 17
0432            0040        7757                7757 ]
0433            0041    #2C LDA i               1020 ]
0434            0042        LZE                 0452 |
0435            0043        BSE i 6             1626 |  Set up proper LZE order to
0436            0044        STC 2L              4444 ]  check link bit results
0437            0045    [   CLR                 0011    Clear link bit
0440            0046    |   LDA 3               1003
0441            0047    [#2X 0                  0000    SCR i order
0442            0050        SAE i 4             1464
0443            0051        HLT                 0000    ACC error
0444            0052    #2L 0                   0000    LZE or LZE i order
0445            0053        HLT                 0000    Error. Link bit
0446            0054        LDA i               1020 ]
0447            0055        1                   0001 |
0450            0056        ADM                 1140 |  Increment shift count
0451            0057        2X                  0441 ]
0452            0060        XSK i 5             0225 ]  Do 20 counts
0453            0061        JMP 2C              6433 ]
0454            0062        LDA i               1020 ]
0455            0063        20                  0020 |
0456            0064        ADM                 1140 |  Increment test constant address
0457            0065        3                   0003 ]
0460            0066        XSK i 2             0222 ]  Do 14 patterns
0461            0067        JMP 2B              6426 ]
0462            0070        XSK i 1             0221
0463            0071        JMP 2A              6416
0464            0072        JMP 1T              6034
0465            0073    #2T 3777                3777 ]
0466            0074        1777                1777 |  Test constants and test results
0467            0075        777                 0777 |
0470            0076        377                 0377 |
0471            0077        177                 0177 ]
```

Test constants and test results

0472	0100	77	0077
0473	0101	37	0037
0474	0102	17	0017
0475	0103	7	0007
0476	0104	3	0003
0477	0105	1	0001
0500	0106	0	0000
0501	0107	0	0000
0502	0110	0	0000
0503	0111	0	0000
0504	0112	0	0000
0505	0113	5777	5777
0506	0114	6777	6777
0507	0115	7377	7377
0510	0116	7577	7577
0511	0117	7677	7677
0512	0120	7737	7737
0513	0121	7757	7757
0514	0122	7767	7767
0515	0123	7773	7773
0516	0124	7775	7775
0517	0125	7776	7776
0520	0126	7777	7777
0521	0127	7777	7777
0522	0130	7777	7777
0523	0131	7777	7777
0524	0132	7777	7777
0525	0133	6777	6777
0526	0134	7377	7377
0527	0135	7577	7577
0530	0136	7677	7677
0531	0137	7737	7737
0532	0140	7757	7757
0533	0141	7767	7767
0534	0142	7773	7773
0535	0143	7775	7775
0536	0144	7776	7776
0537	0145	7777	7777
0540	0146	7777	7777
0541	0147	7777	7777
0542	0150	7777	7777
0543	0151	7777	7777
0544	0152	7777	7777
0545	0153	7377	7377
0546	0154	7577	7577
0547	0155	7677	7677
0550	0156	7737	7737
0551	0157	7757	7757
0552	0160	7767	7767
0553	0161	7773	7773
0554	0162	7775	7775
0555	0163	7776	7776
0556	0164	7777	7777
0557	0165	7777	7777
0560	0166	7777	7777
0561	0167	7777	7777
0562	0170	7777	7777
0563	0171	7777	7777
0564	0172	7777	7777
0565	0173	7577	7577
0566	0174	7677	7677
0567	0175	7737	7737
0570	0176	7757	7757
0571	0177	7767	7767

Test cconstants and test results

0572	0200	7773	7773
0573	0201	7775	7775
0574	0202	7776	7776
0575	0203	7777	7777
0576	0204	7777	7777
0577	0205	7777	7777
0600	0206	7777	7777
0601	0207	7777	7777
0602	0210	7777	7777
0603	0211	7777	7777
0604	0212	7777	7777
0605	0213	7677	7677
0606	0214	7737	7737
0607	0215	7757	7757
0610	0216	7767	7767
0611	0217	7773	7773
0612	0220	7775	7775
0613	0221	7776	7776
0614	0222	7777	7777
0615	0223	7777	7777
0616	0224	7777	7777
0617	0225	7777	7777
0620	0226	7777	7777
0621	0227	7777	7777
0622	0230	7777	7777
0623	0231	7777	7777
0624	0232	7777	7777
0625	0233	7737	7737
0626	0234	7757	7757
0627	0235	7767	7767
0630	0236	7773	7773
0631	0237	7775	7775
0632	0240	7776	7776
0633	0241	7777	7777
0634	0242	7777	7777
0635	0243	7777	7777
0636	0244	7777	7777
0637	0245	7777	7777
0640	0246	7777	7777
0641	0247	7777	7777
0642	0250	7777	7777
0643	0251	7777	7777
0644	0252	7777	7777
0645	0253	7757	7757
0646	0254	7767	7767
0647	0255	7773	7773
0650	0256	7775	7775
0651	0257	7776	7776
0652	0260	7777	7777
0653	0261	7777	7777
0654	0262	7777	7777
0655	0263	7777	7777
0656	0264	7777	7777
0657	0265	7777	7777
0660	0266	7777	7777
0661	0267	7777	7777
0662	0270	7777	7777
0663	0271	7777	7777
0664	0272	7777	7777
0665	0273	7767	7767
0666	0274	7773	7773
0667	0275	7775	7775
0670	0276	7776	7776
0671	0277	7777	7777

Test constants and test results

```
0672    0300          7777          7777
0673    0301          7777          7777
0674    0302          7777          7777
0675    0303          7777          7777
0676    0304          7777          7777
0677    0305          7777          7777
0700    0306          7777          7777
0701    0307          7777          7777
0702    0310          7777          7777
0703    0311          7777          7777
0704    0312          7777          7777
0705    0313          7773          7773
0706    0314          7775          7775
0707    0315          7776          7776
0710    0316          7777          7777
0711    0317          7777          7777
0712    0320          7777          7777
0713    0321          7777          7777
0714    0322          7777          7777
0715    0323          7777          7777
0716    0324          7777          7777
0717    0325          7777          7777
0720    0326          7777          7777
0721    0327          7777          7777
0722    0330          7777          7777
0723    0331          7777          7777
0724    0332          7777          7777
0725    0333          7775          7775
0726    0334          7776          7776
0727    0335          7777          7777
0730    0336          7777          7777
0731    0337          7777          7777
0732    0340          7777          7777
0733    0341          7777          7777
0734    0342          7777          7777
0735    0343          7777          7777
0736    0344          7777          7777
0737    0345          7777          7777
0740    0346          7777          7777
0741    0347          7777          7777
0742    0350          7777          7777
0743    0351          7777          7777
0744    0352          7777          7777
0745    0353          7776          7776
0746    0354          7777          7777
0747    0355          7777          7777
0750    0356          7777          7777
0751    0357          7777          7777
0752    0360          7777          7777
0753    0361          7777          7777
0754    0362          7777          7777
0755    0363          7777          7777
0756    0364          7777          7777
0757    0365          7777          7777
0760    0366          7777          7777
0761    0367          7777          7777
0762    0370          7777          7777
0763    0371          7777          7777
0764    0372          7777          7777
        0373    =1000
1000    0374    #3T   0             0000    i bit for LZE order
1001    0375          i             0020
1002    0376          i             0020
1003    0377          i             0020
```

```
1004    0400    i    0020
1005    0401    i    0020
1006    0402    i    0020    i bit for LZE order
1007    0403    i    0020
1010    0404    i    0020
1011    0405    i    0020
1012    0406    i    0020
1013    0407    i    0020
1014    0410    0    0000
1015    0411    0    0000
1016    0412    0    0000
1017    0413    0    0000
1020    0414    0    0000
1021    0415    i    0020
1022    0416    i    0020
1023    0417    i    0020
1024    0420    i    0020
1025    0421    i    0020
1026    0422    i    0020
1027    0423    i    0020
1030    0424    i    0020
1031    0425    i    0020
1032    0426    i    0020
1033    0427    0    0000
1034    0430    i    0020
1035    0431    i    0020
1036    0432    i    0020
1037    0433    i    0020
1040    0434    0    0000
1041    0435    i    0020
1042    0436    i    0020
1043    0437    i    0020
1044    0440    i    0020
1045    0441    i    0020
1046    0442    i    0020
1047    0443    i    0020
1050    0444    i    0020
1051    0445    i    0020
1052    0446    0    0000
1053    0447    i    0020
1054    0450    i    0020
1055    0451    i    0020
1056    0452    i    0020
1057    0453    i    0020
1060    0454    0    0000
1061    0455    i    0020
1062    0456    i    0020
1063    0457    i    0020
1064    0460    i    0020
1065    0461    i    0020
1066    0462    i    0020
1067    0463    i    0020
1070    0464    i    0020
1071    0465    0    0000
1072    0466    i    0020
1073    0467    i    0020
1074    0470    i    0020
1075    0471    i    0020
1076    0472    i    0020
1077    0473    i    0020
1100    0474    0    0000
1101    0475    i    0020
1102    0476    i    0020
1103    0477    i    0020
```

```
1104    0500        i       0020
1105    0501        i       0020
1106    0502        i       0020    i bit for LZE order
1107    0503        i       0020
1110    0504        0       0000
1111    0505        i       0020
1112    0506        i       0020
1113    0507        i       0020
1114    0510        i       0020
1115    0511        i       0020
1116    0512        i       0020
1117    0513        i       0020
1120    0514        0       0000
1121    0515        i       0020
1122    0516        i       0020
1123    0517        i       0020
1124    0520        i       0020
1125    0521        i       0020
1126    0522        i       0020
1127    0523        0       0000
1130    0524        i       0020
1131    0525        i       0020
1132    0526        i       0020
1133    0527        i       0020
1134    0530        i       0020
1135    0531        i       0020
1136    0532        i       0020
1137    0533        i       0020
1140    0534        0       0000
1141    0535        i       0020
1142    0536        i       0020
1143    0537        i       0020
1144    0540        i       0020
1145    0541        i       0020
1146    0542        0       0000
1147    0543        i       0020
1150    0544        i       0020
1151    0545        i       0020
1152    0546        i       0020
1153    0547        i       0020
1154    0550        i       0020
1155    0551        i       0020
1156    0552        i       0020
1157    0553        i       0020
1160    0554        0       0000
1161    0555        i       0020
1162    0556        i       0020
1163    0557        i       0020
1164    0560        i       0020
1165    0561        0       0000
1166    0562        i       0020
1167    0563        i       0020
1170    0564        i       0020
1171    0565        i       0020
1172    0566        i       0020
1173    0567        i       0020
1174    0570        i       0020
1175    0571        i       0020
1176    0572        i       0020
1177    0573        i       0020
1200    0574        0       0000
1201    0575        i       0020
1202    0576        i       0020
1203    0577        i       0020
```

```
1204    0600        0       0000    [SCRT4
1205    0601        i       0020
1206    0602        i       0020    i bit for LZE order
1207    0603        i       0020
1210    0604        i       0020
1211    0605        i       0020
1212    0606        i       0020
1213    0607        i       0020
1214    0610        i       0020
1215    0611        i       0020
1216    0612        i       0020
1217    0613        i       0020
1220    0614        0       0000
1221    0615        i       0020
1222    0616        i       0020
1223    0617        0       0000
1224    0620        i       0020
1225    0621        i       0020
1226    0622        i       0020
1227    0623        i       0020
1230    0624        i       0020
1231    0625        i       0020
1232    0626        i       0020
1233    0627        i       0020
1234    0630        i       0020
1235    0631        i       0020
1236    0632        i       0020
1237    0633        i       0020
1240    0634        0       0000
1241    0635        i       0020
1242    0636        0       0000
1243    0637        i       0020
1244    0640        i       0020
1245    0641        i       0020
1246    0642        i       0020
1247    0643        i       0020
1250    0644        i       0020
1251    0645        i       0020
1252    0646        i       0020
1253    0647        i       0020
1254    0650        i       0020
1255    0651        i       0020
1256    0652        i       0020
1257    0653        i       0020
1260    0654        0       0000
1261    0655        0       0000
1262    0656        i       0020
1263    0657        i       0020
1264    0660        i       0020
1265    0661        i       0020
1266    0662        i       0020
1267    0663        i       0020
1270    0664        i       0020
1271    0665        i       0020
1272    0666        i       0020
1273    0667        i       0020
1274    0670        i       0020
1275    0671        i       0020
1276    0672        i       0020
1277    0673        i       0020
```

```
                0001    [ADDT1
                0002    [ADD TEST 1
                0003    ⊟400
0400            0004        26                  0026    Test number
0401            0005    #2S SET i 1             0061    Do test 100 times
0402            0006        7677                7677
0403            0007   [#2A CLR                 0011
0404            0010    [   ADD 2K              2450
0405            0011        SAE i               1460
0406            0012        0                   0000
0407            0013        HLT                 0000    Error. 0000 + 0000 = 0000
0410            0014    [   CLR                 0011
0411            0015    [   ADD 3K              2451
0412            0016        SAE i               1460
0413            0017        7777                7777
0414            0020        HLT                 0000    Error. 0000 + 7777 = 7777
0415            0021    [   CLR                 0011
0416            0022    [   COM                 0017
0417            0023    [   ADD 2K              2450
0420            0024        SAE i               1460
0421            0025        7777                7777
0422            0026        HLT                 0000    Error. 7777 + 0000 = 7777
0423            0027    [   CLR                 0011
0424            0030    [   ADD 3K              2451
0425            0031    [   ADD 3K              2451
0426            0032        SAE i               1460
0427            0033        7777                7777
0430            0034        HLT                 0000    Error. 7777 + 7777 = 7777
0431            0035    [   CLR                 0011
0432            0036    [   COM                 0017
0433            0037    [   ADD 4K              2452
0434            0040        SAE i               1460
0435            0041        1                   0001
0436            0042        HLT                 0000    Error. 7777 + 0001 = 0001
0437            0043    [   CLR                 0011
0440            0044    [   ADD 4K              2452
0441            0045    [   ADD 3K              2451
0442            0046        SAE i               1460
0443            0047        1                   0001
0444            0050        HLT                 0000    Error. 0001 + 7777 = 0001
0445            0051        XSK i 1             0221
0446            0052        JMP 2A              6403
0447            0053        JMP 1T              6034    To next test
0450            0054    #2K 0                   0000
0451            0055    #3K 7777                7777
0452            0056    #4K 1                   0001
```

```
                0001    [FADRT1
                0002    [FULL ADDR
                0003    [TEST 1
                0004    [TESTS Q 2,3
                0005    ■400
0400            0006        27                  0027  Test number
0401            0007    #2S SET i 1             0061  Do test 10 times
0402            0010        7767                7767
0403            0011    #2A LDA i               1020
0404            0012        STC 1000            5000
0405            0013        STA                 1040
0406            0014        2C                  0431  Store orders which will be
0407            0015        LDA i               1020  changed
0410            0016        JMP 1000            7000
0411            0017        STA                 1040
0412            0020        3C                  0435
0413            0021        SET i 2             0062
0414            0022        6777                6777
0415            0023        SET i 3             0063
0416            0024        777                 0777  Clear QN 2, 3
0417            0025        CLR                 0011
0420            0026        STA i 3             1063
0421            0027        XSK i 2             0222
0422            0030        JMP P-2             6420
0423            0031        SET i 2             0062  Count 2 quarters
0424            0032        6777                6777
0425            0033        SET i 3             0063  Restore 0
0426            0034        777                 0777
0427            0035    #2B CLR                 0011
0430            0036        ADD 2K              2455  Store JMP 0 in 1000 + i
0431            0037    #2C STC 1000            5000
0432            0040        SAE i               1460
0433            0041        0                   0000
0434            0042        HLT                 0000  Error. ACC ≠ o after STC
0435            0043    #3C JMP 1000            7000  To JMP 0
0436            0044        CLR                 0011  Should return here thru 0
0437            0045        STA i 3             1063  Clear 1000 + i
0440            0046        LDA i               1020
0441            0047        1                   0001
0442            0050        ADM                 1140
0443            0051        2C                  0431
0444            0052        LDA i               1020  Increment addresses
0445            0053        1                   0001
0446            0054        ADM                 1140
0447            0055        3C                  0435
0450            0056        XSK i 2             0222  Do QN 2, 3
0451            0057        JMP 2B              6427
0452            0060        XSK i 1             0221
0453            0061        JMP 2A              6403
0454            0062        JMP 1T              6034  To next test
0455            0063    #2K JMP 0               6000
```

```
                0001    [FADRT2
                0002    [FULL ADDR
                0003    [TEST 2
                0004    [TESTS Q 0, 1
                0005    ⊟400
0400            0006        30                  0030    Test number
0401            0007    #2S LDA i               1020
0402            0010        7767                7767    Set up to do test 10 times
0403            0011        STC 3S              5014
0404            0012        LDA                 1000
0405            0013        1R+1                0021
0406            0014        ADA i               1120    Compute next BN and QN 2
0407            0015        1001                1001
0410            0016        STC P+2             4412
0411            0017        RDC                 0700
0412            0020        0                   0000    Read next block → QN 2
0413            0021        LDA i               1020
0414            0022        1                   0001
0415            0023        ADM                 1140    Add 1 to block increment
0416            0024        1I                  0046    in contrl
0417            0025        JMP 1001            7001    To program
                0026    ⊟1000
1000            0027        30                  0030    Test number
1001            0030        SET i 1             0061
1002            0031        7400                7400
1003            0032        SET i 2             0062
1004            0033        0                   0000
1005            0034        SET i 3             0063
1006            0035        1400                1400    Save QN 0 in QN 3
1007            0036        LDA i 2             1022
1010            0037        STA i 3             1063
1011            0040        XSK i 1             0221
1012            0041        JMP P-3             7007
1013            0042        SET i 1             0061    Do test 10 times
1014            0043    #3S 7767                7767
1015            0044    #2A LDA i               1020
1016            0045        STC 4               4004
1017            0046        STA                 1040
1020            0047        2C                  1043
1021            0050        LDA i               1020    Store orders which will be changed
1022            0051        JMP 4               6004
1023            0052        STA                 1040
1024            0053        3C                  1047
1025            0054        SET i 2             0062
1026            0055        7003                7003
1027            0056        SET i 3             0063
1030            0057        3                   0003    0 → QN 0, 1 except locations 0 - 3
1031            0060        CLR                 0011
1032            0061        STA i 3             1063
1033            0062        XSK i 2             0222
1034            0063        JMP P-2             7032
1035            0064        SET i 2             0062    Count QN 0, 1
1036            0065        7003                7003
1037            0066        SET i 3             0063    To restore 0
1040            0067        3                   0003
1041            0070    [#2B CLR                0011
1042            0071     [  ADD 2K              3101    Store JMP 0 in 4 + i
1043            0072     [#2C STC 4             4004
1044            0073        SAE i               1460
1045            0074        0                   0000
1046            0075        HLT                 0000    Error. ACC ≠ 0 after STC
1047            0076    #3C JMP 4               6004    To JMP 0
1050            0077        CLR                 0011    Should return here thru 0
```

```
1051    0100          STA i 3          1063  [FADRT2   Clear 4 + i    62
1052    0101          LDA i            1020
1053    0102          1                0001
1054    0103          ADM              1140
1055    0104          2C               1043
1056    0105          LDA i            1020  Increment addresses
1057    0106          1                0001
1060    0107          ADM              1140
1061    0110          3C               1047
1062    0111          XSK i 2          0222
1063    0112          JMP 2B           7041  Do QN 0, 1
1064    0113          XSK i 1          0221
1065    0114          JMP 2A           7015
1066    0115          SET i 1          0061
1067    0116          7403             7403
1070    0117          SET i 2          0062
1071    0120          3                0003  Restore contrl to QN 0 from QN 3
1072    0121          SET i 3          0063
1073    0122          1403             1403
1074    0123          LDA i 3          1023
1075    0124          STA i 2          1062
1076    0125          XSK i 1          0221
1077    0126          JMP P-3          7074
1100    0127          JMP 1T           6034  To next test
1101    0130    #2K   JMP 0            6000
```

```
                0001    [iBETA1                                 [iBETA1
                0002    [i-BETA TEST 1
                0003    [i=0
                0004    [BETA=0
                0005    [Q2-Q7
                0006    @400
0400            0007        31                          0031    Test number
0401            0010    #2S SET i 1                     0061 ]
0402            0011        7767                        7767 ]  Do test 10 times
0403            0012    #2A CLR                         0011 ]
0404            0013        ADD 4K                      2454 |  Set up counter for Q2 - Q7
0405            0014        STC 2C                      4451 ]
0406            0015        ADD 6K                      2456 ]
0407            0016        STC 2Z                      4422 |
0410            0017        ADD 7K                      2457 |  Initialize instructions
0411            0020        STC 3Z                      4424 |
0412            0021        ADD 2L                      2460 |
0413            0022        STC 2K                      4452 ]
0414            0023    #2B CLR                         0011 ]
0415            0024        ADD 2K                      2452 |
0416            0025        ADD 3K                      2453 |
0417            0026        STC 2K                      4452 |  Set up test address
0420            0027        ADD 2K                      2452 |
0421            0030        STA                         1040 ]
0422            0031    #2Z 1000                        1000
0423            0032    [   LDA                         1000
0424            0033    [#3Z 1000                       1000
0425            0034        COM                         0017
0426            0035        ADD 2K                      2452
0427            0036        AZE                         0450
0430            0037        HLT                         0000    Error
0431            0040        CLR                         0011
0432            0041        ADD 2Z                      2422 ]
0433            0042        ADD 3K                      2453 |
0434            0043        STC 2Z                      4422 |
0435            0044        ADD 3Z                      2424 |  Increment addresses
0436            0045        ADD 3K                      2453 |
0437            0046        STC 3Z                      4424 ]
0440            0047        ADD 2C                      2451 ]
0441            0050        ADD 5K                      2455 |  Increment counter
0442            0051        STC 2C                      4451 ]
0443            0052        ADD 2C                      2451 ]
0444            0053        APO 1                       0471 ]  Done ?
0445            0054        JMP 2B                      6414    NO
0446            0055        XSK i 1                     0221 ]  YES
0447            0056        JMP 2A                      6403 ]  Do test 10 times
0450            0057        JMP 1T                      6034    To next test
0451            0060    #2C 0                           0000    Counter
0452            0061    #2K 4777                        4777    Current value in test address
0453            0062    #3K 1                           0001
0454            0063    #4K 3000                        3000    Number of locations to test
0455            0064    #5K -1                          7776
0456            0065    #6K 1000                        1000 ]
0457            0066    #7K 1000                        1000 |  Used to initialize instructions
0460            0067    #2L 4777                        4777 ]
```

```
0001    [iBETA2
0002    [i-BETA TEST2
0003    [i=1
0004    [BETA=0
0005    [Q2-Q7
0006    ⊟400
0400 0007       32                  0032    Test number
0401 0010  #2S  SET i 1             0061  ]  Do test 10 times
0402 0011       7767                7767  ]
0403 0012  #2A  CLR                 0011  ]
0404 0013       ADD 4K              2454  |  Set up counter for Q2 - Q7
0405 0014       STC 2C              4451  ]
0406 0015       ADD 6K              2456  ]
0407 0016       STC 2Z              4422  |
0410 0017       ADD 7K              2457  |
0411 0020       STC 3Z              4424  |  Initialize instructions
0412 0021       ADD 2L              2460  |
0413 0022       STC 2K              4452  ]
0414 0023  #2B  CLR                 0011  ]
0415 0024       ADD 2K              2452  |
0416 0025       ADD 3K              2453  |
0417 0026       STC 2K              4452  |  Set up addresses
0420 0027       ADD 2K              2452  |
0421 0030       STA                 1040  |
0422 0031  #2Z  1000                1000  ]
0423 0032  [    LDA i               1020
0424 0033  [#3Z 1000                1000
0425 0034       COM                 0017
0426 0035       ADD 3Z              2424
0427 0036       AZE                 0450
0430 0037       HLT                 0000    Error
0431 0040       CLR                 0011
0432 0041       ADD 2Z              2422  ]
0433 0042       ADD 3K              2453  |
0434 0043       STC 2Z              4422  |
0435 0044       ADD 3Z              2424  |  Increment addresses
0436 0045       ADD 3K              2453  |
0437 0046       STC 3Z              4424  ]
0440 0047       ADD 2C              2451  ]
0441 0050       ADD 5K              2455  |  Increment counter
0442 0051       STC 2C              4451  ]
0443 0052       ADD 2C              2451  ]
0444 0053       APO i               0471  ]  Done ?
0445 0054       JMP 2B              6414    NO
0446 0055       XSK i 1             0221    YES
0447 0056       JMP 2A              6403    Do test 10 times
0450 0057       JMP 1T              6034    To next test
0451 0060  #2C  0                   0000    Counter
0452 0061  #2K  4777                4777    Current value in test address
0453 0062  #3K  1                   0001
0454 0063  #4K  3000                3000    Number of locations to test
0455 0064  #5K  -1                  7776
0456 0065  #6K  1000                1000  ]
0457 0066  #7K  1000                1000  |  Used to initialize instructions
0460 0067  #2L  4777                4777  ]
```

```
                0001    [iBETA3                         [iBETA3
                0002    [i-BETA TEST3
                0003    [i=0
                0004    [BETA=1-17
                0005    [Q2-Q7
                0006    @400
0400            0007        33                  0033    Test number
0401            0010    #2S SET 1 1             0061 ]
0402            0011        7776                7776 ]  Do test 1 time
0403            0012    #2A CLR                 0011 ]
0404            0013        ADD 1               2001 ]  Save register 1
0405            0014        STC 2T              4504 ]
0406            0015        ADD 5L              2520 ]
0407            0016        STC 3C              4506 ]  Set up β counter
0410            0017        ADD 2L              2515 ]
0411            0020        STC 3Z              4442 ]
0412            0021        ADD 3L              2516 ]  Initialize β modification
0413            0022        STC 4Z              4441 ]  instructions
0414            0023    #2B CLR                 0011 ]
0415            0024        ADD 4K              2511 ]  Set up counter for Q2 - Q7
0416            0025        STC 2C              4505 ]
0417            0026        ADD 6K              2513 ]
0420            0027        STC 2Z              4433 ]
0421            0030        ADD 7K              2514 ]  Initialize instructions
0422            0031        STC 2K              4507 ]
0423            0032        ADD 6L              2521 ]
0424            0033        STC 4L              4517 ]
0425            0034    #2D CLR                 0011 ]
0426            0035        ADD 2K              2507 ]
0427            0036        ADD 3K              2510 ]
0430            0037        STC 2K              4507 ]  Set up test address
0431            0040        ADD 2K              2507 ]
0432            0041        STA                 1040 ]
0433            0042    #2Z 1000                1000 ]
0434            0043        CLR                 0011 ]
0435            0044        ADD 4L              2517 ]
0436            0045        ADD 3K              2510 ]
0437            0046        STC 4L              4517 ]  Set up C(β)
0440            0047        ADD 4L              2517 ]
0441            0050    #4Z STC 1               4001 ]
0442            0051    #3Z LDA 1               1001
0443            0052        COM                 0017
0444            0053        ADD 2K              2507
0445            0054        AZE                 0450
0446            0055        HLT                 0000    Error
0447            0056        CLR                 0011
0450            0057        ADD 2Z              2433 ]
0451            0060        ADD 3K              2510 ]  Increment addresses
0452            0061        STC 2Z              4433 ]
0453            0062        ADD 2C              2505 ]
0454            0063        ADD 5K              2512 ]  Increment Q2 - Q7 counter
0455            0064        STC 2C              4505 ]
0456            0065        ADD 2C              2505 ]
0457            0066        APO 1               0471 ]  Done ?
0460            0067        JMP 2D              6425    NO
0461            0070        CLR                 0011 ]  YES
0462            0071        ADD 3Z              2442 ]
0463            0072        ADD 3K              2510 ]  Increment β modification
0464            0073        STC 3Z              4442 ]  instructions
0465            0074        ADD 4Z              2441 ]
0466            0075        ADD 3K              2510 ]
0467            0076        STC 4Z              4441 ]
0470            0077        CLR                 0011 ]
```

```
0471  0100          ADD 3C          2506 ]  [iBETA3
0472  0101          ADD 5K          2512 ]  Increment β counter
0473  0102          STC 3C          4506 ]
0474  0103          ADD 3C          2506 ]  Done ?
0475  0104          APO i           0471 ]
0476  0105          JMP 2B          6414    NO
0477  0106          SET 1           0041 ]  YES
0500  0107          2T              0504 ]
0501  0110          XSK i 1         0221 ]  Do test 1 time
0502  0111          JMP 2A          6403 ]
0503  0112          JMP 1T          6034    To next test
0504  0113    #2T   0               0000    Save register 1
0505  0114    #2C   0               0000    Q2 - Q7 counter
0506  0115    #3C   0               0000    β counter, 1 - 17
0507  0116    #2K   4777            4777    Current value in test address
0510  0117    #3K   1               0001
0511  0120    #4K   3000            3000    Number of addresses to test
0512  0121    #5K   -1              7776
0513  0122    #6K   1000            1000 ]  Used to initialize instructions
0514  0123    #7K   4777            4777 ]
0515  0124    #2L   LDA 1           1001 ]  Used to initialize β mod.
0516  0125    #3L   STC 1           4001 ]  instructions
0517  0126    #4L   777             0777    Current contents of β register
0520  0127    #5L   17              0017    Number of β registers
0521  0130    #6L   777             0777    Initial C(4L)
```

```
0001  [iBETA4
0002  [i-BETA TEST4
0003  [i=1
0004  [BETA=1-17
0005  [Q2-Q7
0006  @400
```

0400	0007	34	0034	Test number
0401	0010	#2S SET i 1	0061	Do test 1 time
0402	0011	7776	7776	
0403	0012	#2A CLR	0011	
0404	0013	ADD 1	2001	Save register 1
0405	0014	STC 2T	4526	
0406	0015	ADD 5L	2542	
0407	0016	STC 3C	4530	Set up β counter
0410	0017	ADD 2L	2537	
0411	0020	STC 3Z	4450	
0412	0021	ADD 3L	2540	Initialize β mod. instruction
0413	0022	STC 4Z	4447	
0414	0023	#2B CLR	0011	Set up counter for Q 2 - Q 7
0415	0024	ADD 4K	2533	
0416	0025	STC 2C	4527	
0417	0026	ADD 6K	2535	
0420	0027	STC 2Z	4433	
0421	0030	ADD 7K	2536	Initialize instruction
0422	0031	STC 2K	4531	
0423	0032	ADD 6L	2543	
0424	0033	STC 4L	4541	
0425	0034	#2D CLR	0011	
0426	0035	ADD 2K	2531	
0427	0036	ADD 3K	2532	
0430	0037	STC 2K	4531	Set up test address
0431	0040	ADD 2K	2531	
0432	0041	STA	1040	
0433	0042	#2Z 1000	1000	
0434	0043	CLR	0011	
0435	0044	ADD 4L	2541	Set up C(β)
0436	0045	COM	0017	
0437	0046	ADD 7L	2544	Currently 1777 ?
0440	0047	AZE	0450	
0441	0050	JMP 2E	6445	NO
0442	0051	CLR	0011	YES
0443	0052	ADD 2M	2545	Make 3777
0444	0053	STC 4L	4541	
0445	0054	#2E CLR	0011	
0446	0055	ADD 4L	2541	Store C(β)
0447	0056	#4Z STC 1	4001	
0450	0057	#3Z LDA i 1	1021	
0451	0060	COM	0017	
0452	0061	ADD 2K	2531	
0453	0062	AZE	0450	
0454	0063	HLT	0000	Error
0455	0064	CLR	0011	
0456	0065	ADD 2Z	2433	
0457	0066	ADD 3K	2532	Increment addresses
0460	0067	STC 2Z	4433	
0461	0070	ADD 4L	2541	
0462	0071	ADD 3K	2532	Increment C(β) for next address
0463	0072	STC 4L	4541	
0464	0073	ADD 4L	2541	
0465	0074	COM	0017	
0466	0075	ADD 3M	2546	At 4000 ?
0467	0076	AZE	0450	
0470	0077	JMP P+4	6474	NO

```
0471  0100          CLR          0011  [iBETA4
0472  0101          ADD 4M       2547    YES
0473  0102          STC 4L       4541    Make 2000
0474  0103          CLR          0011
0475  0104          ADD 2C       2527
0476  0105          ADD 5K       2534    Increment Q 2 - Q 7 counter
0477  0106          STC 2C       4527
0500  0107          ADD 2C       2527    Done ?
0501  0110          APO 1        0471
0502  0111          JMP 2D       6425    NO
0503  0112          CLR          0011    YES
0504  0113          ADD 3Z       2450
0505  0114          ADD 3K       2532
0506  0115          STC 3Z       4450    Increment β mod. instruction
0507  0116          ADD 4Z       2447
0510  0117          ADD 3K       2532
0511  0120          STC 4Z       4447
0512  0121          CLR          0011
0513  0122          ADD 3C       2530
0514  0123          ADD 5K       2534    Increment β counter
0515  0124          STC 3C       4530
0516  0125          ADD 3C       2530    Done ?
0517  0126          APO i        0471
0520  0127          JMP 2B       6414    NO
0521  0130          SET 1        0041    YES
0522  0131          2T           0526
0523  0132          XSK i 1      0221    Do test 1 time
0524  0133          JMP 2A       6403
0525  0134          JMP 1T       6034    To next test
0526  0135    #2T   0            0000    Save register 1
0527  0136    #2C   0            0000    Q 2 - Q 7 counter
0530  0137    #3C   0            0000      counter
0531  0140    #2K   4777         4777    Current value in test address
0532  0141    #3K   1            0001
0533  0142    #4K   3000         3000    Number of memory locations to
0534  0143    #5K   -1           7776    test
0535  0144    #6K   1000         1000    Used to initialize
0536  0145    #7K   4777         4777    instructions
0537  0146    #2L   LDA i 1      1021    Used to initialize β mod.
0540  0147    #3L   STC 1        4001    instructions
0541  0150    #4L   777          0777    Current C(β) before indexing
0542  0151    #5L   17           0017    Number of   register
0543  0152    #6L   777          0777    Initial C(4L)
0544  0153    #7L   1777         1777
0545  0154    #2M   3777         3777
0546  0155    #3M   4000         4000
0547  0156    #4M   2000         2000
```

```
                0001    [LDAT1                          [LDAT1
                0002    [LDA TEST 1
                0003    @400
0400            0004        35                  0035    Test number
0401            0005    #2S SET i 1             0061 ]
0402            0006        7775                7775 ]  Do test 2 times
0403            0007    #2A SET i 2             0062 ]
0404            0010        7773                7773 ]  Do full count in ACC
0405            0011    #2B SET i 3             0063 ]
0406            0012        6000                6000 ]  Do 1777 word segments
0407            0013   [#2C CLR                 0011
0410            0014    |   ADD 2K               2446
0411            0015    |   LDA                  1000
0412            0016    [   3K                   0447
0413            0017        COM                 0017
0414            0020        ADD 4K              2450
0415            0021        AZE                 0450
0416            0022        HLT                 0000    ACC error
0417            0023        CLR                 0011
0420            0024        ADD 3K              2447
0421            0025        COM                 0017
0422            0026        ADD 4K              2450
0423            0027        AZE                 0450
0424            0030        HLT                 0000    C(Y) error
0425            0031        CLR                 0011 ]
0426            0032        ADD 2K              2446 |
0427            0033        ADD 5K              2451 |  Decrease by 1
0430            0034        STC 2K              4446 ]
0431            0035        ADD 3K              2447 ]
0432            0036        ADD 6K              2452 |
0433            0037        STC 3K              4447 |
0434            0040        ADD 4K              2450 |  Increase by 1
0435            0041        ADD 6K              2452 |
0436            0042        STC 4K              4450 ]
0437            0043        XSK i 3             0223 ]  Do 1777 words
0440            0044        JMP 2C              6407 ]
0441            0045        XSK i 2             0222 ]  Do 4 segments
0442            0046        JMP 2B              6405 ]
0443            0047        XSK i 1             0221 ]  Do test 2 times
0444            0050        JMP 2A              6403 ]
0445            0051        JMP 1T              6034    To next test
0446            0052    #2K 7777                7777    Constant in ACC before LDA
0447            0053    #3K 0                   0000    Loaded by LDA
0450            0054    #4K 0                   0000    Duplicate of 3K
0451            0055    #5K -1                  7776
0452            0056    #6K 1                   0001
```

```
0001  [STAT1
0002  [STA TEST 1
0003  ⊟400
0004       36                    0036  Test number
0005  #2S  SET i 1               0061
0006       7775                  7775  Do test -2 times
0007  #2A  SET i 2               0062
0010       7773                  7773  Do full count in ACC
0011  #2B  SET i 3               0063
0012       6000                  6000  Do count in 1777 word segments
0013  #2C  CLR                   0011
0014       ADD 2K                2443
0015       STA                   1040
0016       3K                    0444
0017       COM                   0017
0020       ADD 2K                2443
0021       AZE                   0450
0022       HLT                   0000  ACC error
0023       CLR                   0011
0024       ADD 3K                2444
0025       COM                   0017
0026       ADD 2K                2443
0027       AZE                   0450
0030       HLT                   0000  C(Y) error
0031       CLR                   0011
0032       ADD 2K                2443
0033       ADD 4K                2445  Increment by 1
0034       STC 2K                4443
0035       ADD 3K                2444
0036       ADD 5K                2446  Decrement by 1
0037       STC 3K                4444
0040       XSK i 3               0223
0041       JMP 2C                6407  Do 1777 words
0042       XSK i 2               0222
0043       JMP 2B                6405  Do 4 segments
0044       XSK i 1               0221
0045       JMP 2A                6403  Do test 2 times
0046       JMP 1T                6034  To next test
0047  #2K  0                     0000  Constant in ACC
0050  #3K  7777                  7777  ACC stored here by STA
0051  #4K  1                     0001
0052  #5K  -1                    7776
```

```
                0001    [ADMT1
                0002    [ADM TEST 1
                0003    ⊟400
0400            0004        37                  0037    Test number
0401            0005    #2S SET i 1             0061 ]  Do test 4 times
0402            0006        7773                7773 ]
0403            0007    #2A CLR                 0011 ]
0404            0010        STC 2B+1            4411 ]  Set check counter = 0
0405            0011        SET i 4             0064 ]  Do outer loop 4 times
0406            0012        7773                7773 ]
0407            0013        CLR                 0011
0410            0014    #2B SET i 2             0062 ]  Set check counter
0411            0015        0                   0000 ]
0412            0016        SET i 3             0063 ]  Do inner loop 1777 times
0413            0017        0                   0000 ]
0414            0020    [#3A ADM i              1160 ]  Increment ACC and C(Y)
0415            0021    |   1                   0001 ]
0416            0022    |   XSK i 2             0222 ]  Increment check counter
0417            0023    |   NOP                 0016 ]
0420            0024    |   SAE                 1440
0421            0025    |   2                   0002
0422            0026    |   HLT                 0000    ACC error
0423            0027    |   STC 2T              4452    Save ACC
0424            0030    |   ADD 3A+1            2415
0425            0031    |   SAE                 1440
0426            0032    |   2                   0002
0427            0033    |   HLT                 0000    C(Y) error
0430            0034    |   LDA i               1020 ]
0431            0035    |   1                   0001 ]  Restore C(Y) = 1
0432            0036    |   STC 3A+1            4415 ]
0433            0037    L   ADD 2T              2452    Restore ACC
0434            0040        XSK i 3             0223 ]  Do inner loop
0435            0041        JMP 3A              6414 ]
0436            0042        ADA i               1120 ]  Fix ACC count for next loop
0437            0043        1                   0001 ]
0440            0044        LDA i               1020 ]
0441            0045        2000                2000 ]
0442            0046        ADD 2B+1            2411 ]  Increment bits 11, 10 of
0443            0047        STA                 1040 ]  check counter
0444            0050        2B+1                0411 ]
0445            0051        XSK i 4             0224 ]  Do outer loop
0446            0052        JMP 2B              6410 ]
0447            0053        XSK i 1             0221 ]  Do test 4 times
0450            0054        JMP 2A              6403 ]
0451            0055        JMP 1T              6034    To next test
0452            0056    #2T 0                   0000    ACC temporary storage
```

```
                0001    [LAMT1
                0002    [LAM TEST 1
                0003    ⊟400
0400            0004        40              0040    Test number
0401            0005    #2S SET i 1         0061    Do test 40 times
0402            0006        7737            7737
0403            0007    #2A SET i 7         0067    Do 11 test conditions
0404            0010        7766            7766
0405            0011        SET i 2         0062    Initial C(ACC)
0406            0012        2T-1            0444
0407            0013        SET i 3         0063    Initial C(link bit)
0410            0014        3T-1            0455
0411            0015        SET i 4         0064    Initial C(Y)
0412            0016        4T-1            0466
0413            0017        SET i 5         0065    Final C(ACC) and C(Y)
0414            0020        5T-1            0477
0415            0021        SET i 6         0066    Final C(link bit)
0416            0022        6T-1            0510
0417            0023    [#2B LDA i 4        1024    Set up initial C(Y)
0420            0024        STC 7T          4522
0421            0025        LDA i 6         1026    Final C(link bit) test
0422            0026        STC 2Z          4436    instruction
0423            0027        LDA i 3         1023
0424            0030        ROL i 1         0261    Initial C(link bit)
0425            0031        LDA i 2         1022    Initial C(ACC)
0426            0032        LAM             1200
0427            0033        7T              0522
0430            0034        SAE i 5         1465
0431            0035        HLT             0000    ACC error
0432            0036        LDA             1000
0433            0037        7T              0522
0434            0040        SAE 5           1445
0435            0041        HLT             0000    C(Y) error
0436            0042    #2Z 0               0000    C(link bit) test instruction
0437            0043        HLT             0000    C(link bit) error
0440            0044        XSK i 7         0227
0441            0045        JMP 2B          6417    Do 11 test conditions
0442            0046        XSK i 1         0221
0443            0047        JMP 2A          6403    Do test 40 times
0444            0050        JMP 1T          6034    To next test
0445            0051    #2T 0               0000
0446            0052        0               0000
0447            0053        7777            7777
0450            0054        1               0001
0451            0055        0               0000    Initial C(ACC)
0452            0056        7777            7777
0453            0057        7777            7777
0454            0060        0               0000
0455            0061        7777            7777
0456            0062    #3T 0               0000
0457            0063        4000            4000
0460            0064        4000            4000
0461            0065        0               0000
0462            0066        4000            4000    Initial C(link bit)
0463            0067        4000            4000
0464            0070        0               0000
0465            0071        0               0000
0466            0072        0               0000
0467            0073    #4T 0               0000
0470            0074        0               0000
0471            0075        0               0000    Initial C(Y)
0472            0076        7777            7777
0473            0077        7777            7777
```

```
0474  0100          7777          7777  [LAMT1
0475  0101          0             0000    Initial C(Y)
0476  0102          7777          7777
0477  0103          7777          7777
0500  0104    #5T   0             0000
0501  0105          1             0001
0502  0106          0             0000
0503  0107          0             0000
0504  0110          0             0000    Final C(ACC) and C(Y)
0505  0111          7777          7777
0506  0112          7777          7777
0507  0113          7777          7777
0510  0114          7776          7776
0511  0115    #6T   LZE           0452
0512  0116          LZE           0452
0513  0117          LZE  i        0472
0514  0120          LZE  i        0472    Final C(link bit) test
0515  0121          LZE  i        0472      instruction
0516  0122          LZE  i        0472
0517  0123          LZE           0452
0520  0124          LZE           0452
0521  0125          LZE  i        0472
0522  0126    #7T   0             0000    Active memory location
```

```
                0001    [MULT1
                0002    [MUL TEST 1
                0003    ⊟400
0400    0041    0004        41                  0041    Test number
0401    0042    0005    #2S SET i 1             0061
0402    0043    0006        7767                7767    Do test 10 times
0403    0044    0007    #2A CLR                 0011
0404    0045    0010        STC 2K              4470    Clear C(ACC) test quantity
0405    0046    0011        SET i 2             0062
0406    0047    0012        2T-1                0472    Fraction multiply result
0407    0050    0013        SET i 3             0063
0410    0051    0014        3T-1                0572    Integer multiply result
0411    0052    0015        SET i 4             0064
0412    0053    0016        7767                7767    Do 10 groups of ACC test quantity
0413    0054    0017    #2B CLR                 0011
0414    0055    0020        STC 3K              4471    Clear C(Y) test quantity
0415    0056    0021        SET i 5             0065
0416    0057    0022        7767                7767    Do 10 counts of C(Y) test quantity
0417    0060    0023    [#2C LDA                1000
0420    0061    0024     |  2K                 0470
0421    0062    0025     |  MUL                1240    Fraction multiply
0422    0063    0026     L  4000+3K             4471
0423    0064    0027        SAE i 2             1462
0424    0065    0030        HLT                 0000    ACC error
0425    0066    0031        APO                 0451
0426    0067    0032        JMP P+4             6432
0427    0070    0033        LZE                 0452
0430    0071    0034        HLT                 0000    Error. C(ACC) = +; C(link bit) = 1
0431    0072    0035        JMP P+3             6434
0432    0073    0036        LZE i               0472
0433    0074    0037        HLT                 0000    Error. C(ACC) = -; C(link bit) = 0
0434    0075    0040    [   LDA                 1000
0435    0076    0041     |  2K                 0470
0436    0077    0042     |  MUL                1240    Integer multiply
0437    0100    0043     L  3K                 0471
0440    0101    0044        SAE i 3             1463
0441    0102    0045        HLT                 0000    ACC error
0442    0103    0046        APO                 0451
0443    0104    0047        JMP P+4             6447
0444    0105    0050        LZE                 0452
0445    0106    0051        HLT                 0000    Error. C(ACC) = +; C(link bit) = 1
0446    0107    0052        JMP P+3             6451
0447    0110    0053        LZE i               0472
0450    0111    0054        HLT                 0000    Error. C(ACC) = -; C(link bit) = 0
0451    0112    0055        LDA                 1000
0452    0113    0056        3K                  0471
0453    0114    0057        ADD 4K              2472    Increment C(Y) test quantity
0454    0115    0060        STC 3K              4471
0455    0116    0061        XSK i 5             0225    Do 10 counts of C(Y) test quantity
0456    0117    0062        JMP 2C              6417
0457    0120    0063        LDA                 1000
0460    0121    0064        2K                  0470
0461    0122    0065        ADD 4K              2472    Increment C(ACC) test quantity
0462    0123    0066        STC 2K              4470
0463    0124    0067        XSK i 4             0224    Do 10 groups of C(ACC) test constant
0464    0125    0070        JMP 2B              6413
0465    0126    0071        XSK i 1             0221    Do test 10 times
0466    0127    0072        JMP 2A              6403
0467    0130    0073        JMP 1T              6034    To next test
0470    0131    0074    #2K 0                   0000    C(ACC) test quantity
0471    0132    0075    #3K 0                   0000    C(Y) test quantity
0472    0133    0076    #4K 1111                1111    Incrementing constant
0473    0134    0077    #2T 0                   0000
```

```
0474    0100            0       0000    [MULT1
0475    0101            0       0000
0476    0102            0       0000    Fraction multiply results
0477    0103            7777    7777
0500    0104            7777    7777
0501    0105            7777    7777
0502    0106            7777    7777
0503    0107            0       0000
0504    0110            247     0247
0505    0111            516     0516
0506    0112            765     0765
0507    0113            7012    7012
0510    0114            7261    7261
0511    0115            7530    7530
0512    0116            7777    7777
0513    0117            0       0000
0514    0120            516     0516
0515    0121            1234    1234
0516    0122            1752    1752
0517    0123            6025    6025
0520    0124            6543    6543
0521    0125            7261    7261
0522    0126            7777    7777
0523    0127            0       0000
0524    0130            765     0765
0525    0131            1752    1752
0526    0132            2737    2737
0527    0133            5040    5040
0530    0134            6025    6025
0531    0135            7012    7012
0532    0136            7777    7777
0533    0137            7777    7777
0534    0140            7012    7012
0535    0141            6025    6025
0536    0142            5040    5040
0537    0143            2737    2737
0540    0144            1752    1752
0541    0145            765     0765
0542    0146            0       0000
0543    0147            7777    7777
0544    0150            7261    7261
0545    0151            6543    6543
0546    0152            6025    6025
0547    0153            1752    1752
0550    0154            1234    1234
0551    0155            516     0516
0552    0156            0       0000
0553    0157            7777    7777
0554    0160            7530    7530
0555    0161            7261    7261
0556    0162            7012    7012
0557    0163            765     0765
0560    0164            516     0516
0561    0165            247     0247
0562    0166            0       0000
0563    0167            7777    7777
0564    0170            7777    7777
0565    0171            7777    7777
0566    0172            7777    7777
0567    0173            0       0000
0570    0174            0       0000
0571    0175            0       0000
0572    0176            0       0000
0573    0177    #3T     0       0000    Integer multiply results
```

0574	0200	0	0000	[MULT1
0575	0201	0	0000	
0576	0202	0	0000	Integer multiply results
0577	0203	7777	7777	
0600	0204	7777	7777	
0601	0205	7777	7777	
0602	0206	7777	7777	
0603	0207	0	0000	
0604	0210	321	0321	
0605	0211	642	0642	
0606	0212	1163	1163	
0607	0213	6614	6614	
0610	0214	7135	7135	
0611	0215	7456	7456	
0612	0216	7777	7777	
0613	0217	0	0000	
0614	0220	642	0642	
0615	0221	1504	1504	
0616	0222	2346	2346	
0617	0223	5431	5431	
0620	0224	6273	6273	
0621	0225	7135	7135	
0622	0226	7777	7777	
0623	0227	0	0000	
0624	0230	1163	1163	
0625	0231	2346	2346	
0626	0232	3531	3531	
0627	0233	4246	4246	
0630	0234	5431	5431	
0631	0235	6614	6614	
0632	0236	7777	7777	
0633	0237	7777	7777	
0634	0240	6614	6614	
0635	0241	5431	5431	
0636	0242	4246	4246	
0637	0243	3531	3531	
0640	0244	2346	2346	
0641	0245	1163	1163	
0642	0246	0	0000	
0643	0247	7777	7777	
0644	0250	7135	7135	
0645	0251	6273	6273	
0646	0252	5431	5431	
0647	0253	2346	2346	
0650	0254	1504	1504	
0651	0255	642	0642	
0652	0256	0	0000	
0653	0257	7777	7777	
0654	0260	7456	7456	
0655	0261	7135	7135	
0656	0262	6614	6614	
0657	0263	1163	1163	
0660	0264	642	0642	
0661	0265	321	0321	
0662	0266	0	0000	
0663	0267	7777	7777	
0664	0270	7777	7777	
0665	0271	7777	7777	
0666	0272	7777	7777	
0667	0273	0	0000	
0670	0274	0	0000	
0671	0275	0	0000	
0672	0276	0	0000	

```
                0001    [SROT1                          [SROT1
                0002    [SRO TEST 1
                0003    ⊟400
0400            0004        42                  0042    Test number
0401            0005    #2S SET i 1             0061    Do test 2 times
0402            0006        7775                7775
0403            0007    #2A CLR                 0011    Clear test quantity
0404            0010        STC 2T              4470
0405            0011        SET i 2             0062    Outer loop
0406            0012        7677                7677
0407            0013    #2B SET i 3             0063    Inner loop
0410            0014        7677                7677
0411            0015    #2E LDA                 1000
0412            0016        2T                  0470
0413            0017        ROR 1               0301    Simulate rotate part
0414            0020        STA                 1040
0415            0021        3T                  0471
0416            0022        APO                 0451    Skip ?
0417            0023        JMP 2C              6427    NO
0420            0024        LDA i               1020    YES
0421            0025        HLT                 0000
0422            0026        STC 2Z+2            4443    Set up check for skip
0423            0027        LDA i               1020
0424            0030        NOP                 0016
0425            0031        STC 2Z+3            4444
0426            0032        JMP 2D              6435
0427            0033    #2C LDA i               1020    No skip
0430            0034        JMP 2X              6445
0431            0035        STC 2Z+2            4443
0432            0036        LDA i               1020    Set up check for no skip
0433            0037        HLT                 0000
0434            0040        STC 2Z+3            4444
0435            0041    [#2D ADD 2T             2470
0436            0042     |  STC 4T             4472
0437            0043     |  LDA i              1020
0440            0044     |  7777               7777
0441            0045     |  #2Z SRO            1500
0442            0046     [     4T               0472
0443            0047        NOP                 0016    Error. Did not skip
0444            0050        NOP                 0016    Error. Skipped
0445            0051    #2X SAE i               1460
0446            0052        7777                7777
0447            0053        HLT                 0000    Error. ACC changed
0450            0054        LDA                 1000
0451            0055        4T                  0472
0452            0056        SAE                 1440
0453            0057        3T                  0471
0454            0060        HLT                 0000    Error. Memory not rotated
0455            0061        LDA i               1020    properly
0456            0062        1                   0001
0457            0063        ADM                 1140    Increment test quantity
0460            0064        2T                  0470
0461            0065        XSK i 3             0223    Do inner loop
0462            0066        JMP 2E              6411
0463            0067        XSK i 2             0222    Do outer loop
0464            0070        JMP 2B              6407
0465            0071        XSK i 1             0221    Do test 2 times
0466            0072        JMP 2A              6403
0467            0073        JMP 1T              6034    To next test
0470            0074    #2T 0                   0000    Test constant
0471            0075    #3T 0                   0000    Simulated answer
0472            0076    #4T 0                   0000    Actual answer
```

```
                0001    [SETT1
                0002    [SET TEST 1
                0003    [i=0
                0004    ⊟400
0400            0005         43                  0043    Test number
0401            0006    #2S  JMP  .+2            6403    Do test 1 time
0402            0007         7776                7776
0403            0010    #2A  LDA  i              1020
0404            0011         SET  0              0040
0405            0012         STC  2X             4416    Initialize β modification
0406            0013         LDA  i              1020    instructions
0407            0014         0                   0000
0410            0015         STC  2Z             4433
0411            0016    #2B  CLR                 0011
0412            0017         STC  2K             4473    Clear test values
0413            0020         STC  3K             4474
0414            0021    [#2C LDA  i              1020
0415            0022         7777                7777
0416            0023    [#2X SET  0              0040
0417            0024         2K                  0473
0420            0025         SAE  i              1460
0421            0026         7777                7777
0422            0027         HLT                 0000    Error C(ACC) changed
0423            0030         LDA                 1000
0424            0031         2K                  0473
0425            0032         SAE                 1440
0426            0033         3K                  0474
0427            0034         HLT                 0000    Error C(Y) changed
0430            0035         LDA                 1000
0431            0036         3K                  0474
0432            0037         SAE                 1440
0433            0040    #2Z  0                   0000
0434            0041         HLT                 0000    Error. C(β) not correct
0435            0042         LDA                 1000
0436            0043         3K                  0474    Count 0 - 7777 through ?
0437            0044         SAE  i              1460
0440            0045         7777                7777
0441            0046         JMP  2D             6460    NO
0442            0047         LDA                 1000    YES
0443            0050         2Z                  0433
0444            0051         SAE  i              1460    Through 0 - 17 β register ?
0445            0052         17                  0017
0446            0053         JMP  2E             6465    NO
0447            0054         LDA                 1000    YES
0450            0055         2S+1                0402
0451            0056         ADD  4K             2475
0452            0057         STA                 1040    Do test 1 time
0453            0060         2S+1                0402
0454            0061         SAE  i              1460
0455            0062         7777                7777
0456            0063         JMP  2A             6403
0457            0064         JMP  1T             6034    To next test
0460            0065    #2D  ADD  4K             2475    Not through 0 - 7777 count
0461            0066         STA                 1040
0462            0067         3K                  0474    Increase counts in 2K and 3K
0463            0070         STC  2K             4473
0464            0071         JMP  2C             6414
0465            0072    #2E  ADD  4K             2475
0466            0073         STC  2Z             4433    Not through 0 - 17 β register
0467            0074         ADD  2X             2416
0470            0075         ADD  4K             2475    Increase β modification
0471            0076         STC  2X             4416    instructions
0472            0077         JMP  2B             6411
```

```
0473    0100    #2K 0           0000    [SETT1  Value stored into C(β)
0474    0101    #3K 0           0000     Duplicate of 2K
0475    0102    #4K 1           0001
```

```
                0001    [SETT2
                0002    [SET TEST 2
                0003    [i=1
                0004    ■400
0400            0005        44              0044    Test number
0401            0006    #2S JMP P+2         6403    Do test 1 time
0402            0007        7776            7776
0403            0010    #2A LDA i           1020
0404            0011        SET i 0         0060
0405            0012        STC 2X          4416    Initialize β modification
0406            0013        LDA i           1020    instructions
0407            0014        0               0000
0410            0015        STC 2Z          4433
0411            0016    #2B CLR             0011
0412            0017        STC 2K          4417    Clear test values
0413            0020        STC 3K          4473
0414            0021    [#2C LDA i          1020
0415            0022    [   7777            7777
0416            0023    [#2X SET i 0        0060
0417            0024    [#2K 0              0000
0420            0025        SAE i           1460
0421            0026        7777            7777
0422            0027        HLT             0000    Error. C(ACC) changed
0423            0030        LDA             1000
0424            0031        2K              0417
0425            0032        SAE             1440
0426            0033        3K              0473
0427            0034        HLT             0000    Error. C(Y) changed
0430            0035        LDA             1000
0431            0036        3K              0473
0432            0037        SAE             1440
0433            0040    #2Z 0               0000
0434            0041        HLT             0000    Error. C(β) not correct
0435            0042        LDA             1000
0436            0043        3K              0473    Count 0 - 7777 through ?
0437            0044        SAE i           1460
0440            0045        7777            7777
0441            0046        JMP 2D          6460    NO
0442            0047        LDA             1000    YES
0443            0050        2Z              0433    Through 0 - 17 β register ?
0444            0051        SAE i           1460
0445            0052        17              0017
0446            0053        JMP 2E          6465    NO
0447            0054        LDA             1000    YES
0450            0055        2S+1            0402
0451            0056        ADD 4K          2474
0452            0057        STA             1040    Do test 1 time
0453            0060        2S+1            0402
0454            0061        SAE i           1460
0455            0062        7777            7777
0456            0063        JMP 2A          6403
0457            0064        JMP 1T          6034    To next test
0460            0065    #2D ADD 4K          2474    Not through 0 - 7777 count
0461            0066        STA             1040
0462            0067        3K              0473    Increase count in 2K and 3K
0463            0070        STC 2K          4417
0464            0071        JMP 2C          6414
0465            0072    #2E ADD 4K          2474    Not through 0 - 17 β register
0466            0073        STC 2Z          4433
0467            0074        ADD 2X          2416
0470            0075        ADD 4K          2474    Increase β modification
0471            0076        STC 2X          4416    instruction
0472            0077        JMP 2B          6411
```

```
0473    0100    #3K 0                   0000    [SETT2  Value stored into C(β)
0474    0101    #4K 1                   0001
```

```
                0001    [XSKT1
                0002    [XSK TEST 1
                0003    [i=0
                0004    @400
0400            0005        45          0045    Test number
0401            0006    #2S JMP P+2     6403    Do test 1 time
0402            0007        7776        7776
0403            0010    #2A LDA i       1020
0404            0011        SET i 1     0061
0405            0012        STC 2X      4444
0406            0013        LDA i       1020    Initialize β modification
0407            0014        1           0001    instructions
0410            0015        STC 2Z      4457
0411            0016        LDA i       1020
0412            0017        XSK 1       0201
0413            0020        STC 2Y      4446
0414            0021    #2B CLR         0011    Clear test values
0415            0022        STC 2K      4445
0416            0023    #2H LDA         1000
0417            0024        2K          0445    Check for address part of
0420            0025        BCL i       1560    C(β) = 1777
0421            0026        6000        6000
0422            0027        SAE i       1460
0423            0030        1777        1777
0424            0031        JMP 2C      6434    NO
0425            0032        LDA i       1020    YES
0426            0033        HLT         0000
0427            0034        STC 2Y+1    4447
0430            0035        LDA i       1020    Set up checks for skips
0431            0036        NOP         0016
0432            0037        STC 2Y+2    4450
0433            0040        JMP 2D      6442
0434            0041    #2C LDA i       1020
0435            0042        JMP 2Y+3    6451
0436            0043        STC 2Y+1    4447    Set up check for no skips
0437            0044        LDA i       1020
0440            0045        HLT         0000
0441            0046        STC 2Y+2    4450
0442            0047    #2D LDA i       1020    Initialize C(ACC)
0443            0050        7777        7777
0444            0051    #2X SET i 1     0061    Initialize C(β)
0445            0052    #2K 0           0000
0446            0053    #2Y XSK 1       0201
0447            0054        NOP         0016    Error. Did not skip
0450            0055        NOP         0016    Error. Skipped
0451            0056        SAE i       1460
0452            0057        7777        7777
0453            0060        HLT         0000    Error. C(ACC) changed
0454            0061        LDA         1000
0455            0062        2K          0445
0456            0063        SAE         1440
0457            0064    #2Z 1           0001
0460            0065        HLT         0000    Error. C(β) not correct
0461            0066        LDA         1000
0462            0067        2K          0445    Count 0 - 7777 through ?
0463            0070        SAE i       1460
0464            0071        7777        7777
0465            0072        JMP 2E      6504    NO
0466            0073        LDA         1000    YES
0467            0074        2Z          0457
0470            0075        SAE i       1460    Through 1 - 17 β registers ?
0471            0076        17          0017
0472            0077        JMP 2F      6510    NO
```

```
0473  0100          LDA          1000  ] [XSKT1
0474  0101          2S+1         0402  ]  YES
0475  0102          ADD 4K       2521  |
0476  0103          STA          1040  |  Do test 1 time
0477  0104          2S+1         0402  |
0500  0105          SAE i        1460  |
0501  0106          7777         7777  |
0502  0107          JMP 2A       6403  ]
0503  0110          JMP 1T       6034     To next test
0504  0111    #2E   ADD 4K       2521  ]  Not through 0 - 7777 count
0505  0112          STA          1040  |
0506  0113          2K           0445  |  Increase test values
0507  0114          JMP 2H       6416  ]
0510  0115    #2F   ADD 4K       2521  ]  Not through 1 - 17 β register
0511  0116          STC 2Z       4457  |
0512  0117          ADD 2X       2444  |
0513  0120          ADD 4K       2521  |
0514  0121          STC 2X       4444  |  Increase β modification
0515  0122          ADD 2Y       2446  |  instruction
0516  0123          ADD 4K       2521  |
0517  0124          STC 2Y       4446  |
0520  0125          JMP 2B       6414  ]
0521  0126    #4K   1            0001
```

```
                0001    [XSKT2
                0002    [XSK TEST 2
                0003    [i=1
                0004    ⊟400
0400            0005        46                  0046    Test number
0401            0006    #2S JMP P+2             6403    Do test 1 time
0402            0007        7776                7776
0403            0010    #2A LDA i               1020
0404            0011        SET i 1             0061
0405            0012        STC 2X              4463
0406            0013        LDA i               1020    Initialize β modification
0407            0014        1                   0001    instructions
0410            0015        STC 2Z              4476
0411            0016        LDA i               1020
0412            0017        XSK i 1             0221
0413            0020        STC 2Y              4465
0414            0021    #2B CLR                 0011
0415            0022        STC 2K              4464    Clear test values
0416            0023        STC 3K              4540
0417            0024    #2H LDA                 1000
0420            0025        2K                  0464
0421            0026        BCL i               1560    Compute C(β) after indexing
0422            0027        6000                6000
0423            0030        ADD 4K              2541
0424            0031        BCL i               1560
0425            0032        6000                6000
0426            0033        STC 3K              4540
0427            0034        ADD 2K              2464
0430            0035        BCL i               1560
0431            0036        1777                1777
0432            0037        BSE                 1600
0433            0040        3K                  0540    Check for address part of
0434            0041        STC 3K              4540    C(β) = 1777
0435            0042        LDA                 1000
0436            0043        3K                  0540
0437            0044        BCL i               1560
0440            0045        6000                6000
0441            0046        SAE i               1460
0442            0047        1777                1777
0443            0050        JMP 2C              6453    NO
0444            0051        LDA i               1020    YES
0445            0052        HLT                 0000
0446            0053        STC 2Y+1            4466
0447            0054        LDA i               1020    Set up check for skip
0450            0055        NOP                 0016
0451            0056        STC 2Y+2            4467
0452            0057        JMP 2D              6461
0453            0060    #2C LDA i               1020
0454            0061        JMP 2Y+3            6470
0455            0062        STC 2Y+1            4466
0456            0063        LDA i               1020    Set up check for no skip
0457            0064        HLT                 0000
0460            0065        STC 2Y+2            4467
0461            0066    #2D LDA i               1020    Initialize C(ACC)
0462            0067        7777                7777
0463            0070    #2X SET i 1             0061    Initialize C(β)
0464            0071    #2K 0                   0000
0465            0072    #2Y XSK i 1             0221
0466            0073        NOP                 0016    Error. Did not skip
0467            0074        NOP                 0016    Error. Skipped
0470            0075        SAE i               1460
0471            0076        7777                7777
0472            0077        HLT                 0000    Error. C(ACC) changed
```

```
0473  0100        LDA       1000
0474  0101        3K        0540
0475  0102        SAE       1440
0476  0103  #2Z   1         0001
0477  0104        HLT       0000   Error. C(β) not correct
0500  0105        LDA       1000
0501  0106        2K        0464   Count 0 - 7777 through ?
0502  0107        SAE i     1460
0503  0110        7777      7777
0504  0111        JMP 2E    6523   NO
0505  0112        LDA       1000   YES
0506  0113        2Z        0476
0507  0114        SAE i     1460   Through 1 - 17 β register ?
0510  0115        17        0017
0511  0116        JMP 2F    6527   NO
0512  0117        LDA       1000   YES
0513  0120        2S+1      0402
0514  0121        ADD 4K    2541
0515  0122        STA       1040   Do test 1 time
0516  0123        2S+1      0402
0517  0124        SAE i     1460
0520  0125        7777      7777
0521  0126        JMP 2A    6403
0522  0127        JMP 1T    6034   To next test
0523  0130  #2E   ADD 4K    2541   Not through 0 - 7777 count
0524  0131        STA       1040
0525  0132        2K        0464   Increase test values
0526  0133        JMP 2H    6417
0527  0134  #2F   ADD 4K    2541   Not through 1 - 17 β registers
0530  0135        STC 2Z    4476
0531  0136        ADD 2X    2463
0532  0137        ADD 4K    2541
0533  0140        STC 2X    4463   Increase β modification
0534  0141        ADD 2Y    2465   instructions
0535  0142        ADD 4K    2541
0536  0143        STC 2Y    4465
0537  0144        JMP 2B    6414
0540  0145  #3K   0         0000   C(β) after indexing
0541  0146  #4K   1         0001
```

```
                0001    [AZET1                          [AZET1
                0002    [AZE TEST 1
                0003    ⊟400
0400            0004        47                  0047    Test number
0401            0005    #2S SET i 1             0061    Do test 10 times
0402            0006        7767                7767
0403            0007    #2A LDA i               1020
0404            0010        0                   0000
0405            0011        AZE                 0450
0406            0012        HLT                 0000    Error. C(ACC) = 0 and no skip
0407            0013        AZE i               0470
0410            0014        JMP P+2             6412
0411            0015        HLT                 0000    Error. C(ACC) = 0 and skipped
0412            0016        SAE i               1460
0413            0017        0                   0000
0414            0020        HLT                 0000    Error. C(ACC) changed
0415            0021        LDA i               1020
0416            0022        7777                7777
0417            0023        AZE                 0450
0420            0024        HLT                 0000    Error. C(ACC) = -0 and no skip
0421            0025        AZE i               0470
0422            0026        JMP P+2             6424
0423            0027        HLT                 0000    Error. C(ACC) = -0 and skipped
0424            0030        SAE i               1460
0425            0031        7777                7777
0426            0032        HLT                 0000    Error. C(ACC)changed
0427            0033        SET i 2             0062
0430            0034        7747                7747
0431            0035        SET i 3             0063    Do test  for 30 values
0432            0036        2T-1                0447
0433            0037    #2B LDA i 3             1023    Test value → C(ACC)
0434            0040        AZE i               0470
0435            0041        HLT                 0000    Error. C(ACC) ≠ 0 and no skip
0436            0042        AZE                 0450
0437            0043        JMP P+2             6441
0440            0044        HLT                 0000    Error. C(ACC) ≠ 0 and skipped
0441            0045        SAE 3               1443
0442            0046        HLT                 0000    Error. C(ACC) changed
0443            0047        XSK i 2             0222
0444            0050        JMP 2B              6433    Do 30 test values
0445            0051        XSK i 1             0221
0446            0052        JMP 2A              6403    Do test 10 times
0447            0053        JMP 1T              6034    To next test
0450            0054    #2T 7776                7776
0451            0055        7775                7775
0452            0056        7773                7773
0453            0057        7767                7767
0454            0060        7757                7757
0455            0061        7737                7737    Floating 0
0456            0062        7677                7677
0457            0063        7577                7577
0460            0064        7377                7377
0461            0065        6777                6777
0462            0066        5777                5777
0463            0067        3777                3777
0464            0070        1                   0001
0465            0071        2                   0002
0466            0072        4                   0004
0467            0073        10                  0010
0470            0074        20                  0020    Floating 1
0471            0075        40                  0040
0472            0076        100                 0100
0473            0077        200                 0200
```

```
0474    0100    400     0400 | [AZET1
0475    0101    1000    1000 |
0476    0102    2000    2000 |
0477    0103    4000    4000 ]
```

```
                0001    [APOT1
                0002    [APO TEST 1
                0003    ⊟400
0400    0004            50                  0050    Test number
0401    0005    #2S     SET i 1             0061    ┐ Do test 10 times
0402    0006            7767                7767    ┘
0403    0007    #2A     SET i 2             0062    ┐
0404    0010            7762                7762    │ Do 15 positive patterns
0405    0011            SET i 3             0063    │
0406    0012            2T-1                0441    ┘
0407    0013    #2B     LDA i 3             1023    ┐
0410    0014            APO                 0451    │
0411    0015            HLT                 0000    │ Error. C(ACC) positive and
0412    0016            APO i               0471    ┘ no skip
0413    0017            JMP P+2             6415
0414    0020            HLT                 0000    Error. C(ACC) positive and skip
0415    0021            SAE 3               1443
0416    0022            HLT                 0000    Error. C(ACC) changed
0417    0023            XSK i 2             0222    ┐ Do 15 positive patterns
0420    0024            JMP 2B              6407    ┘
0421    0025            SET i 2             0062    ┐
0422    0026            7762                7762    │
0423    0027            SET i 3             0063    │ Do 15 negative patterns
0424    0030            3T-1                0456    ┘
0425    0031    #2C     LDA i 3             1023    ┐
0426    0032            APO i               0471    │
0427    0033            HLT                 0000    │ Error. C(ACC) negative and no
0430    0034            APO                 0451    ┘ skip
0431    0035            JMP P+2             6433
0432    0036            HLT                 0000    Error. C(ACC) negative and
0433    0037            SAE 3               1443    skip
0434    0040            HLT                 0000    Error. C(ACC) changed
0435    0041            XSK i 2             0222    ┐ Do 15 negative patterns
0436    0042            JMP 2C              6425    ┘
0437    0043            XSK i 1             0221    ┐ Do test 10 times
0440    0044            JMP 2A              6403    ┘
0441    0045            JMP 1T              6034    To next test
0442    0046    #2T     0                   0000    ┐
0443    0047            1                   0001    │
0444    0050            2                   0002    │
0445    0051            4                   0004    │
0446    0052            10                  0010    │
0447    0053            20                  0020    │ Positive patterns
0450    0054            40                  0040    │
0451    0055            100                 0100    │
0452    0056            200                 0200    │
0453    0057            400                 0400    │
0454    0060            1000                1000    │
0455    0061            2000                2000    │
0456    0062            3777                3777    ┘
0457    0063    #3T     7777                7777    ┐
0460    0064            7776                7776    │
0461    0065            7775                7775    │
0462    0066            7773                7773    │ Negative patterns
0463    0067            7767                7767    │
0464    0070            7757                7757    │
0465    0071            7737                7737    │
0466    0072            7677                7677    │
0467    0073            7577                7577    │
0470    0074            7377                7377    │
0471    0075            6777                6777    │
0472    0076            5777                5777    │
0473    0077            4000                4000    ┘
```

```
                0001    [LZET1
                0002    [LZE TEST 1
                0003    ⊟400
0400            0004        51                  0051    Test number
0401            0005    #2S SET i 1             0061 ]  Do test 10 times
0402            0006        7767                7767 ]
0403            0007    #2A SET i 2             0062 ]
0404            0010        7745                7745 |  Do 32 patterns in C(ACC) with
0405            0011        SET i 3             0063 |  C(L) = 0
0406            0012        2T-1                0455 ]
0407            0013    [#2B LDA i              1020 ]
0410            0014    |   0                   0000 |  0 → C(L)
0411            0015    |   ROL i 1             0261 ]
0412            0016    |   LDA i 3             1023
0413            0017    [   LZE                 0452
0414            0020        HLT                 0000    Error. C(L) = 0 and no skip
0415            0021        LZE i               0472
0416            0022        JMP P+2             6420
0417            0023        HLT                 0000    Error. C(L) = 0 and skipped
0420            0024        SAE 3               1443
0421            0025        HLT                 0000    Error. C(ACC) changed
0422            0026        ROR i 1             0321
0423            0027        APO                 0451
0424            0030        HLT                 0000    Error. C(L) ≠ 0
0425            0031        XSK i 2             0222 ]  Do 32 patterns
0426            0032        JMP 2B              6407 ]
0427            0033        SET i 2             0062 ]
0430            0034        7745                7745 |  Do 32 patterns in C(ACC)
0431            0035        SET i 3             0063 |  with C(L) = 1
0432            0036        2T-1                0455 ]
0433            0037    [#2C LDA i              1020 ]
0434            0040    |   4000                4000 |  1 → C(L)
0435            0041    |   ROL i 1             0261 ]
0436            0042    |   LDA i 3             1023
0437            0043    [   LZE i               0472
0440            0044        HLT                 0000    Error. C(L) = 1 and no skip
0441            0045        LZE                 0452
0442            0046        JMP P+2             6444
0443            0047        HLT                 0000    Error. C(L) = 1 and skipped
0444            0050        SAE 3               1443
0445            0051        HLT                 0000    Error. C(L) ≠ 1
0446            0052        ROR i 1             0321
0447            0053        APO i               0471
0450            0054        HLT                 0000
0451            0055        XSK i 2             0222 ]  Do 32 patterns
0452            0056        JMP 2C              6433 ]
0453            0057        XSK i 1             0221 ]  Do test 10 times
0454            0060        JMP 2A              6403 ]
0455            0061        JMP 1T              6034    To next test
0456            0062    #21 0                   0000 ]
0457            0063        1                   0001 |
0460            0064        2                   0002 |
0461            0065        4                   0004 |
0462            0066        10                  0010 |
0463            0067        20                  0020 |
0464            0070        40                  0040 |
0465            0071        100                 0100 |  Floating 1
0466            0072        200                 0200 |
0467            0073        400                 0400 |
0470            0074        1000                1000 |
0471            0075        2000                2000 |
0472            0076        4000                4000 ]
0473            0077        7777                7777 ]
```

0474	0100	7776	7776	[LZET1
0475	0101	7775	7775	
0476	0102	7773	7773	
0477	0103	7767	7767	
0500	0104	7757	7757	
0501	0105	7737	7737	
0502	0106	7677	7677	Floating 0
0503	0107	7577	7577	
0504	0110	7377	7377	
0505	0111	6777	6777	
0506	0112	5777	5777	
0507	0113	3777	3777	

```
                0001    [HWCT1
                0002    [HALF WORD
                0003    [CLASS TEST 1
                0004    [i = 0
                0005    [BETA = 0
                0006    ⊟400
0400            0007        52                  0052    Test number
0401            0010        SET i 1             0061
0402            0011        7767                7767    Do test 10 times
0403            0012    #2N CLR                 0011
0404            0013        ADD 4A              2477 ┐
0405            0014        STC 4B              4500 │
0406            0015        ADD 4C              2501 │
0407            0016        STC 2E              4431 │
0410            0017        ADD 4C              2501 │  Initialize storage locations
0411            0020        STC 3E              4433 │
0412            0021        ADD 4D              2502 │
0413            0022        STC 2D              4426 │
0414            0023        ADD 4D              2502 │
0415            0024        STC 3D              4437 │
0416            0025        STC 2A              4473 ┘
0417            0026    #2M CLR                 0011
0420            0027        ADD 2A              2473 ┐
0421            0030        ADD 2B              2474 │  Set up pattern to be stored
0422            0031        ADD 2C              2475 │
0423            0032        STC 2A              4473 │
0424            0033        ADD 2A              2473 ┘
0425            0034        STH                 1340 ┐
0426            0035    #2D 5000                5000 │
0427            0036        ROR 6               0306 │
0430            0037        STH                 1340 │
0431            0040    #2E 1000                1000 │  Store pattern,
0432            0041        LDH                 1300 │  load pattern, and
0433            0042    #3E 1000                1000 │  compare
0434            0043        ROL 6               0246 │
0435            0044        STC 4E              4503 │
0436            0045        LDH                 1300 │
0437            0046    #3D 5000                5000 │
0440            0047        ADD 4E              2503 │
0441            0050        COM                 0017 │
0442            0051        ADD 2A              2473 │
0443            0052        AZE                 0450 ┘
0444            0053        HLT                 0000    Error
0445            0054        CLR                 0011
0446            0055        ADD 2D              2426 ┐
0447            0056        ADD 2F              2476 │
0450            0057        STC 2D              4426 │
0451            0060        ADD 3D              2437 │
0452            0061        ADD 2F              2476 │  Go to next memory address
0453            0062        STC 3D              4437 │
0454            0063        ADD 2E              2431 │
0455            0064        ADD 2F              2476 │
0456            0065        STC 2E              4431 │
0457            0066        ADD 3E              2433 │
0460            0067        ADD 2F              2476 │
0461            0070        STC 3E              4433 │
0462            0071        ADD 4B              2500 │
0463            0072        ADD 2B              2474 │
0464            0073        STC 4B              4500 │
0465            0074        ADD 4B              2500 ┘
0466            0075        APO i               0471 ┐  Done all memory ?
0467            0076        JMP 2M              6417 ┘
0470            0077        XSK i 1             0221
```

```
0471    0100          JMP 2N          6403   [HWCT1 Do again
0472    0101          JMP 34          6034   Go on to next program
0473    0102    #2A   0               0000
0474    0103    #2B   -1              7776
0475    0104    #2C   100             0100
0476    0105    #2F   1               0001
0477    0106    #4A   3000            3000
0500    0107    #4B   0               0000
0501    0110    #4C   1000            1000
0502    0111    #4D   5000            5000
0503    0112    #4E   0               0000
```

```
                0001    [HWCT2
                0002    [HALF WORD
                0003    [CLASS TEST 2
                0004    [i=1
                0005    [BETA=0
                0006    @400
0400            0007        53                  0053
0401            0010        SET i 1             0061    Test number
0402            0011        7767                7767    Do test 10 times
0403            0012    #2A CLR                 0011
0404            0013        ADD 4A              2474
0405            0014        STC 4B              4475
0406            0015        ADD 3A              2465    Initialize storage locations
0407            0016        STC 2B              4430
0410            0017        ADD 3A              2465
0411            0020        STC 2D              4435
0412            0021        ADD 3B              2466
0413            0022        STC 2C              4433
0414            0023        STC 3C              4467
0415            0024    #2E CLR                 0011
0416            0025        ADD 3C              2467
0417            0026        ADD 3D              2470    Set up pattern
0420            0027        ADD 3F              2472
0421            0030        STC 3C              4467
0422            0031        LDA                 1000
0423            0032        2B                  0430
0424            0033        SCR 6               0346
0425            0034        STC 3G              4473
0426            0035        ADD 3C              2467
0427            0036        STH                 1340
0430            0037    #2B0                    0000    Store pattern
0431            0040        ROR 6               0306
0432            0041        STH                 1340
0433            0042    #2C                     0000
0434            0043        LDH i               1320
0435            0044    #2D                     0000
0436            0045        COM                 0017
0437            0046        ADD 3G              2473    Load pattern and check
0440            0047        AZE                 0450
0441            0050        HLT                 0000    Error
0442            0051        CLR                 0011
0443            0052        ADD 2B              2430
0444            0053        ADD 3E              2471
0445            0054        STC 2B              4430
0446            0055        ADD 2C              2433
0447            0056        ADD 3E              2471    Go to next memory address
0450            0057        STC 2C              4433
0451            0060        ADD 2D              2435
0452            0061        ADD 3E              2471
0453            0062        STC 2D              4435
0454            0063        ADD 4B              2475
0455            0064        ADD 3D              2470
0456            0065        STC 4B              4475
0457            0066        ADD 4B              2475
0460            0067        APO i               0471
0461            0070        JMP 2E              6415
0462            0071        XSK i 1             0221
0463            0072        JMP 2A              6403
0464            0073        JMP 34              6034
0465            0074    #3A 1000                1000
0466            0075    #3B 5000                5000
0467            0076    #3C                     0000
0470            0077    #3D -1                  7776
```

```
0471    0100    #3E 1           0001    [HWCT2
0472    0101    #3F 100         0100
0473    0102    #3G             0000
0474    0103    #4A 3000        3000
0475    0104    #4B             0000
```

```
                0001    [HWCT3
                0002    [HALF WORD
                0003    [CLASS
                0004    [TEST 3
                0005    [i=0
                0006    [BETA=1-17
                0007    =400
0400            0010        54                  0054    Test number
0401            0011        SET 1 1             0061
0402            0012        7776                7776
0403            0013    #2A CLR                 0011
0404            0014        ADD 1               2001
0405            0015        STC 2B              4544
0406            0016        ADD 5A              2563
0407            0017        STC 5B              4564
0410            0020    #2L CLR                 0011
0411            0021        ADD 3A              2552
0412            0022        STC 2K              4551
0413            0023        ADD 4A              2556
0414            0024        STC 4B              4557
0415            0025        LDA                 1000
0416            0026        2D                  0545
0417            0027        STA                 1040
0420            0030        2H                  0455
0421            0031        STA                 1040
0422            0032        2H+6                0463
0423            0033        STA                 1040
0424            0034        2H+12               0467    Start with β = 1
0425            0035        LDA                 1000
0426            0036        2E                  0546
0427            0037        STA                 1040
0430            0040        2H+3                0460
0431            0041        STA                 1040
0432            0042        2H+7                0464
0433            0043        LDA                 1000
0434            0044        2F                  0547
0435            0045        STA                 1040
0436            0046        2H+5                0462
0437            0047        STA                 1040
0440            0050        2H+14               0471
0441            0051        STA                 1040
0442            0052        2J                  0453
0443            0053        LDA                 1000
0444            0054        2G                  0550
0445            0055        STA                 1040
0446            0056        2H+10               0465
0447            0057        STA                 1040
0450            0060        2H+15               0472
0451            0061        CLR                 0011
0452            0062        ADD 2K              2551
0453            0063    #2J STC1                4001
0454            0064        CLR                 0011
0455            0065    #2H ADD 1               2001    Store address plus 4000 at
0456            0066        ADD 4C              2560    each memory location
0457            0067        ROR 6               0306
0460            0070        STH 1               1341
0461            0071        ROL 6               0246
0462            0072        STC 1               4001
0463            0073        ADD 1               2001
0464            0074        STH 1               1341
0465            0075        LDH 1               1301
0466            0076        STC 4E              4562
0467            0077        ADD 1               2001
```

```
0470  0100          ADD 4D          2561   [HWCT3
0471  0101          STC 1           4001
0472  0102          LDH 1           1301
0473  0103          ROL 6           0246
0474  0104          ADD 4E          2562
0475  0105          COM             0017
0476  0106          ADD 2K          2551
0477  0107          ADD 4C          2560
0500  0110          AZE             0450   Check pattern stored
0501  0111          HLT             0000   Error
0502  0112          CLR             0011
0503  0113          ADD 2K          2551   ]
0504  0114          ADD 3E          2555   |
0505  0115          STC 2K          4551   |
0506  0116          ADD 4B          2557   |  Go to next address
0507  0117          ADD 3D          2554   |
0510  0120          STC 4B          4557   |
0511  0121          ADD 4B          2557   ]
0512  0122          APO 1           0471
0513  0123          JMP 2J-2        6451
0514  0124          CLR             0011
0515  0125          ADD 2D          2545   ]
0516  0126          ADD 3E          2555   |
0517  0127          STC 2D          4545   |
0520  0130          ADD 2E          2546   |
0521  0131          ADD 3E          2555   |
0522  0132          STC 2E          4546   |  Go to next β register
0523  0133          ADD 2F          2547   |
0524  0134          ADD 3E          2555   |
0525  0135          STC 2F          4547   |
0526  0136          ADD 2G          2550   |
0527  0137          ADD 3E          2555   |
0530  0140          STC 2G          4550   |
0531  0141          ADD 5B          2564   |
0532  0142          ADD 3D          2554   |
0533  0143          STC 5B          4564   ]
0534  0144          ADD 5B          2564
0535  0145          APO 1           0471
0536  0146          JMP 2L          6410
0537  0147          SET 1           0041
0540  0150          2B              0544
0541  0151          XSK 1 1         0221
0542  0152          JMP 2A          6403
0543  0153          JMP 34          6034
0544  0154    #2B                   0000
0545  0155    #2D ADD 1             2001
0546  0156    #2E STH 1             1341
0547  0157    #2F STC 1             4001
0550  0160    #2G LDH 1             1301
0551  0161    #2K                   0000
0552  0162    #3A 1000              1000
0553  0163    #3C                   0000
0554  0164    #3D -1                7776
0555  0165    #3E 1                 0001
0556  0166    #4A 3000              3000
0557  0167    #4B                   0000
0560  0170    #4C 4000              4000
0561  0171    #4D -4000             3777
0562  0172    #4E                   0000
0563  0173    #5A 17                0017
0564  0174    #5B                   0000
```

```
                0001    [HWCT4                          [HWCT4
                0002    [HALF WORD
                0003    [CLASS TEST 4
                0004    [i = 1
                0005    [BETA = 1-17
                0006    ■400
0400            0007        55                  0055    Test number
0401            0010        SET i 1             0061
0402            0011        7776                7776
0403            0012    #2A CLR                 0011
0404            0013        ADD 1               2001
0405            0014        STC 2B              4573
0406            0015        ADD 5A              2571
0407            0016        STC 5B              4572
0410            0017        LDA i               1020 ┐
0411            0020        STC 1               4001 │
0412            0021        STC 2F              4574 │  Initialize instructions
0413            0022        LDA i               1020 │
0414            0023        STH i 1             1361 │
0415            0024        STC 2G              4575 │
0416            0025        LDA i               1020 │
0417            0026        LDH i 1             1321 │
0420            0027        STC 2H              4576 │
0421            0030        LDA i               1020 │
0422            0031        ADD 1               2001 │
0423            0032        STC 2J              4577 ┘
0424            0033    #2Q CLR                 0011
0425            0034        ADD 5B              2572
0426            0035        ADD 4F              2606
0427            0036        STC 5B              4572
0430            0037        LDA                 1000 ┐
0431            0040        2F                  0574 │
0432            0041        STA                 1040 │
0433            0042        6A                  0464 │
0434            0043        STA                 1040 │
0435            0044        6D                  0477 │
0436            0045        STA                 1040 │
0437            0046        6H                  0523 │
0440            0047        LDA                 1000 │
0441            0050        2G                  0575 │  Start with β = 1
0442            0051        STA                 1040 │
0443            0052        6B                  0472 │
0444            0053        STA                 1040 │
0445            0054        6C                  0474 │
0446            0055        LDA                 1000 │
0447            0056        2H                  0576 │
0450            0057        STA                 1040 │
0451            0060        6E                  0500 │
0452            0061        STA                 1040 │
0453            0062        6F                  0503 │
0454            0063        LDA                 1000 │
0455            0064        2J                  0577 │
0456            0065        STA                 1040 │
0457            0066        6G                  0550 ┘
0460            0067        CLR                 0011
0461            0070        ADD 4C              2603
0462            0071        STC 2C              4600
0463            0072        ADD 2C              2600
0464            0073    #6A                     0000
0465            0074        ADD 4D              2604
0466            0075        STC 2D              4601
0467            0076    #2L ADD 2D              2601
0470            0077        ADD 4E              2605
```

```
0471  0100          ROR 6          0306
0472  0101  #6B                   0000
0473  0102          ROL 6          0246
0474  0103  #6C                   0000
0475  0104          CLR            0011
0476  0105          ADD 2C         2600
0477  0106  #6D                   0000
0500  0107  #6E                   0000
0501  0110          ROL 6          0246
0502  0111          STC 2E         4602
0503  0112  #6F                   0000
0504  0113          ADD 2E         2602
0505  0114          COM            0017
0506  0115          ADD 2D         2601
0507  0116          ADD 4E         2605
0510  0117          AZE            0450   Check pattern stored
0511  0120          HLT            0000   Error
0512  0121          CLR            0011
0513  0122          ADD 2D         2601
0514  0123          SAE            1440 ┐
0515  0124          4G             0607 │
0516  0125          JMP 2K         6530 │
0517  0126          CLR            0011 │
0520  0127          ADD 4H         2610 │
0521  0130          STC 2C         4600 │  Go to second memory
0522  0131          ADD 2C         2600 │
0523  0132  #6H                   0000 │
0524  0133          ADD 2D         2601 │
0525  0134          ADD 4F         2606 │
0526  0135          STC 2D         4601 │
0527  0136          JMP 2L         6467 ┘
0530  0137  #2K SAE               1440 ┐
0531  0140          4J             0611 │
0532  0141          JMP 2M         6544 │
0533  0142          CLR            0011 │
0534  0143          ADD 5B         2572 │  Go to next β register
0535  0144          AZE            0450 │
0536  0145          JMP 2N         6553 ┘
0537  0146          SET 1          0041 ┐
0540  0147          2B             0573 │  Do test ? times
0541  0150          XSK 1 1        0221 │
0542  0151          JMP 2A         6403 ┘
0543  0152          JMP 34         6034
0544  0153  #2M CLR                0011
0545  0154          ADD 2D         2601
0546  0155          ADD 4F         2606
0547  0156          STC 2D         4601
0550  0157  #6G                   0000
0551  0160          STC 2C         4600
0552  0161          JMP 2L         6467
0553  0162  #2N LDA                1000 ┐
0554  0163          2F             0574 │
0555  0164          ADD 4F         2606 │
0556  0165          STC 2F         4574 │
0557  0166          ADD 2G         2575 │  Increment β instructions
0560  0167          ADD 4F         2606 │
0561  0170          STC 2G         4575 │
0562  0171          ADD 2H         2576 │
0563  0172          ADD 4F         2606 │
0564  0173          STC 2H         4576 │
0565  0174          ADD 2J         2577 │
0566  0175          ADD 4F         2606 │
0567  0176          STC 2J         4577 │
0570  0177          JMP 2Q         6424 │
```

```
0571    0200    #5A -17          7760   CHWCT4
0572    0201    #5B              0000
0573    0202    #2B              0000
0574    0203    #2F              0000
0575    0204    #2G              0000
0576    0205    #2H              0000
0577    0206    #2J              0000
0600    0207    #2C              0000   Current memory address
0601    0210    #2D              0000
0602    0211    #2E              0000
0603    0212    #4C 4777         4777
0604    0213    #4D 1000         1000
0605    0214    #4E 4000         4000
0606    0215    #4F 1            0001
0607    0216    #4G 1777         1777
0610    0217    #4H 7777         7777
0611    0220    #4J 3777         3777
```

```
                0001    [HWCT5
                0002    [SKIP IF HALF
                0003    [DIFFERS
                0004    @400
0400            0005        56                  0056    Test number
0401            0006        SET i 1             0061
0402            0007        7677                7677
0403            0010    #2A LDA i               1020
0404            0011        0077                0077
0405            0012        SHD i               1420        Proper patterns
0406            0013        7700                7700
0407            0014        JMP P+2             6411
0410            0015        HLT                 0000    Error. RH(A) = 77; LH(Y) = 77
0411            0016        LDA i               1020
0412            0017        0077                0077
0413            0020        SHD i               1420
0414            0021        0077                0077
0415            0022        HLT                 0000    Error. RH(A) = 77; LH(Y) = 00
0416            0023        LDA i               1020
0417            0024        7700                7700
0420            0025        SHD i               1420
0421            0026        0077                0077
0422            0027        JMP P+2             6424
0423            0030        HLT                 0000    Error. RH(A) = 00; LH(Y) = 00
0424            0031        LDA i               1020
0425            0032        7700                7700
0426            0033        SHD i               1420
0427            0034        7700                7700
0430            0035        HLT                 0000    Error. RH(A) = 00; LH(Y) = 77
0431            0036        SET i 3             0063
0432            0037        -16                 7761
0433            0040        SET i 2             0062
0434            0041        3A-1                0574
0435            0042    #2B LDA i 2             1022
0436            0043        SHD 2               1402
0437            0044        HLT                 0000    Error. RH(A) ≠ LH(3A)
0440            0045        CLR                 0011
0441            0046        ADD 2               2002
0442            0047        ADD 3B              2613
0443            0050        STC 2               4002
0444            0051        LDA 2               1002
0445            0052        SHD 2               1402
0446            0053        JMP P+2             6450
0447            0054        HLT                 0000    Error. RH(A) = RH(3A)
0450            0055        CLR                 0011
0451            0056        ADD 3B              2613
0452            0057        COM                 0017
0453            0060        ADD 2               2002
0454            0061        STC 2               4002
0455            0062        XSK i 3             0223
0456            0063        JMP 2B              6435
0457            0064        SET i 2             0062
0460            0065        3C                  0614
0461            0066        SET i 4             0064
0462            0067        3A-1                0574
0463            0070        SET i 3             0063
0464            0071        -16                 7761
0465            0072    #2C LDA i 4             1024
0466            0073        SHD 2               1402
0467            0074        JMP P+2             6471
0470            0075        HLT                 0000    Error. RH(A) = LH(3C)
0471            0076        CLR                 0011
0472            0077        ADD 2               2002
```

```
0473  0100          ADD 3B          2613
0474  0101          STC 2           4002
0475  0102          LDA 4           1004
0476  0103          SHD 2           1402
0477  0104          HLT             0000    Error. RH(A) ≠ RH(3C)
0500  0105          CLR             0011
0501  0106          ADD 3B          2613
0502  0107          COM             0017
0503  0110          ADD 2           2002
0504  0111          ADD 3D          2632
0505  0112          STC 2           4002
0506  0113          XSK 1 3         0223
0507  0114          JMP 2C          6465
0510  0115          SET 1 3         0063
0511  0116          -16             7761
0512  0117          SET 1 2         0062
0513  0120          3A-4000         4574
0514  0121          SET 1 4         0064
0515  0122          3A-1            0574
0516  0123    #2D   LDA 1 4         1024
0517  0124          SHD 1 2         1422
0520  0125          HLT             0000    Error. RH(A) ≠ LH(3A)
0521  0126          CLR             0011
0522  0127          LDA 4           1004
0523  0130          SHD 1 2         1422
0524  0131          JMP P+2         6526
0525  0132          HLT             0000    Error. RH(A) = RH(3A)
0526  0133          XSK 1 3         0223
0527  0134          JMP 2D          6516
0530  0135          SET 1 3         0063
0531  0136          -16             7761
0532  0137          SET 1 2         0062
0533  0140          3C-4000         4613
0534  0141          SET 1 4         0064
0535  0142          3A-1            0574
0536  0143    #2E   LDA 1 4         1024
0537  0144          SHD 1 2         1422
0540  0145          JMP P+2         6542
0541  0146          HLT             0000    Error. RH(A) = LH(3C)
0542  0147          CLR             0011
0543  0150          LDA 4           1004
0544  0151          SHD 1 2         1422
0545  0152          HLT             0000    Error. RH(A) ≠ RH(3C)
0546  0153          XSK 1 3         0223
0547  0154          JMP 2E          6536
0550  0155          LDA 1           1020
0551  0156          0077            0077
0552  0157          SHD             1400
0553  0160          3E              0633
0554  0161          HLT             0000    Error. RH(A) = 77; LH(3E) = 00
0555  0162          SHD             1400
0556  0163          3E+4000         4633
0557  0164          JMP P+2         6561
0560  0165          HLT             0000    Error. RH(A) = 77; RH(3E) = 77
0561  0166          LDA 1           1020
0562  0167          7700            7700
0563  0170          SHD             1400
0564  0171          3E+1            0634
0565  0172          HLT             0000    Error. RH(A) = 00; LH(3E+1) = 77
0566  0173          SHD             1400
0567  0174          3E+4001         4634
0570  0175          JMP P+2         6572
0571  0176          HLT             0000    Error. RH(A) = 00; RH(3E+1) = 00
0572  0177          XSK 1 1         0221
```

```
0573  0200          JMP 2A          6403  [HWCT5
0574  0201          JMP 34          6034
0575  0202    #3A   0100            0100
0576  0203          0001            0001
0577  0204          0002            0002
0600  0205          0004            0004
0601  0206          0010            0010
0602  0207          0020            0020
0603  0210          0040            0040
0604  0211          0077            0077
0605  0212          0076            0076
0606  0213          0075            0075
0607  0214          0073            0073
0610  0215          0067            0067
0611  0216          0057            0057
0612  0217          0037            0037
0613  0220    #3B   4000            4000
0614  0221    #3C   0010            0010
0615  0222          0100            0100
0616  0223          0200            0200
0617  0224          0400            0400
0620  0225          1000            1000
0621  0226          2000            2000
0622  0227          4000            4000
0623  0230          7700            7700
0624  0231          7600            7600
0625  0232          7500            7500
0626  0233          7300            7300
0627  0234          6700            6700
0630  0235          5700            5700
0631  0236          3700            3700
0632  0237    #3D   1               0001
0633  0240    #3E   0077            0077
0634  0241          7700            7700
```

```
                0001    [RANADD
                0002    [RANDOM ADD
                0003    ■400
0400            0004        57          0057    Program number
0401            0005    #2S SET i 1     0061  ]
0402            0006        7677        7677  ] Do test 100 times
0403            0007    #2A SET i 10    0070
0404            0010        7T-1        0446
0405            0011        SET i 2     0062
0406            0012        7T-2T-1     7767
0407            0013    #2B LDA 3       1003  ]
0410            0014        STA         1040  ] Get random number
0411            0015        4           0004  ]
0412            0016        ADM i 10    1170  ]
0413            0017        ADD 4       2004  ]
0414            0020        STA         1040  ] A + B
0415            0021        3T          0457  ]
0416            0022        COM         0017  ]
0417            0023        STA         1040  ] -A - B
0420            0024        4T          0460  ]
0421            0025        ADA 10      1110  ]
0422            0026        STA         1040  ] -A - B + A = -B
0423            0027        5T          0461  ]
0424            0030        COM         0017  ]
0425            0031        STA         1040  ] -(-B) = B
0426            0032        6T          0462  ]
0427            0033        SAE         1440  ]
0430            0034        4           0004  ] Does C(ACC) = B ?
0431            0035        JMP 2C      6441    NO Check further
0432            0036    #3C SET 3       0043    YES Continue
0433            0037        10          0010
0434            0040        XSK i 2     0222
0435            0041        JMP 2B      6407
0436            0042        XSK i 1     0221    Test done 100 times ?
0437            0043        JMP 2A      6403    NO
0440            0044        JMP 1T      6034    YES To read next test
0441            0045    #2C LDA         1000  ]
0442            0046        4           0004  ] Further check
0443            0047        SAE i       1460  ] C(ACC) ≠ B
0444            0050        7777        7777  ]
0445            0051        HLT         0000  ] Error unless B = -0
0446            0052        JMP 3C      6432  ]
0447            0053    #7T 1234        1234
0450            0054        7106        7106
0451            0055        5502        5502
0452            0056        0132        0132
0453            0057        6714        6714
0454            0060        1055        1055
0455            0061        2135        2135
0456            0062    #2T 3344        3344
0457            0063    #3T 0           0000    A + B
0460            0064    #4T 0           0000    -A - B
0461            0065    #5T 0           0000    -A - B + A = -B
0462            0066    #6T 0           0000    -(-B)=B
```

```
                0001    [ATRT1
                0002    [ATR AND RTA
                0003    [LOGIC PATH
                0004    [TEST ONE
                0005    ⊟400
0400            0006        0060            0060    Test number
0401            0007        SET i 3         0063
0402            0010        7677            7677
0403            0011    #2B SET i 1         0061
0404            0012        7677            7677
0405            0013        SET i 2         0062
0406            0014        0000            0000    Bit pattern
0407            0015    #2C LDA             1000 ┐
0410            0016        2               0002 │
0411            0017        ATR             0014 │  Exchange bit pattern and
0412            0020        CLR             0011 │  check for error
0413            0021        RTA             0015 │
0414            0022        SAE             1440 │
0415            0023        2               0002 ┘
0416            0024        JMP P+7         6425
0417            0025        XSK i 2         0222 ┐  Index and check for end
0420            0026        XSK i 1         0221 │
0421            0027        JMP 2C          6407 │
0422            0030        XSK i 3         0223 ┘
0423            0031        JMP 2B          6403
0424            0032        JMP 2D          6435
0425            0033        ADA i           1120 ┐
0426            0034        100             0100 │
0427            0035        ROL i 6         0266 │  Set link bit and error display
0430            0036        ADA             1100 │
0431            0037        2               0002 │
0432            0040        HLT             0000 ┘
0433            0041        CLR             0011
0434            0042        JMP 2C          6407    Try same pattern
0435            0043    #2D CLR             0011
0436            0044        ATR             0014
0437            0045        JMP 34          6034    Finished
```

```
                0001    [IBZT1
                0002    [INTER-
                0003    [BLOCK
                0004    [ZONE
                0005    [TEST
                0006    @400
0400            0007        61                  0061    Test number
0401            0010        SET i 1             0061
0402            0011        7776                7776
0403            0012    #2A SET i 2             0062 ]  Do test once
0404            0013        7677                7677 ]  200 times through check loop
0405            0014        LDA i               1020
0406            0015        0                   0000    Start at block 0
0407            0016        STC 2C              4424
0410            0017        LDA i               1020
0411            0020        2                   0002    Then do block 2
0412            0021        STC 2D              4436
0413            0022    #2B SET i 11            0071
0414            0023        -40                 7737    Delay to middle of interblock zone
0415            0024        SET i 12            0072
0416            0025        -100                7677
0417            0026        SET i 13            0073
0420            0027        -40                 7737
0421            0030        SET i 14            0074
0422            0031        -100                7677
0423            0032        CHK i               0727
0424            0033    #2C 0                   0000
0425            0034        XSK i 11            0231
0426            0035        JMP P-1             6425
0427            0036        IBZ                 0453
0430            0037        JMP 3A              6467    In zone error
0431            0040        XSK i 12            0232
0432            0041        JMP P-1             6431
0433            0042        IBZ i               0473
0434            0043        JMP 3B              6472    Out of zone
0435            0044        CHK i               0727
0436            0045    #2D 1                   0001
0437            0046        XSK i 13            0233
0440            0047        JMP P-1             6437
0441            0050        IBZ i               0473
0442            0051        JMP P+2             6444
0443            0052        JMP 3C              6475    In zone
0444            0053        XSK i 14            0234
0445            0054        JMP P-1             6444
0446            0055        IBZ                 0453
0447            0056        JMP P+2             6451
0450            0057        JMP 3D              6500    Out of zone
0451            0060        LDA i               1020 ]
0452            0061        4                   0004 |
0453            0062        ADM                 1140 |  Increment check instructions
0454            0063        2C                  0424 |  to do even blocks from 0 to 402
0455            0064        ADA i               1120 |
0456            0065        2                   0002 |
0457            0066        STC 2D              4436 ]
0460            0067        XSK i 2             0222
0461            0070        JMP 2B              6413
0462            0071        XSK i 1             0221
0463            0072        JMP 2A              6403    Do whole test again
0464            0073        CHK                 0707 ]
0465            0074        60                  0060 |  Reposition tape and jump
0466            0075        JMP 34              6034 ]  to control
0467            0076    #3A CHK                 0707
0470            0077        60                  0060
```

```
0471  0100        HLT      0000  [IBZT1  Error.
0472  0101  #3B   CHK      0707  Tape was in zone
0473  0102        60       0060
0474  0103        HLT      0000  Out of zone
0475  0104  #3C   CHK      0707
0476  0105        60       0060
0477  0106        HLT      0000  In zone
0500  0107  #3D   CHK      0707
0501  0110        60       0060
0502  0111        HLT      0000  Out of zone
```

```
0001      [JMPUP
0002      [JUMP TEST
0003      [ONE
0004      [CHECKS
0005      [REGISTERS
0006      [FROM 3A TO
0007      [ 1777 AND
0010      [FROM 3 TO
0011      [377
0012      ⊟400
0400 0013          62          0062    Test number
0401 0014          SET i 1     0061    Do test once
0402 0015          7776        7776
0403 0016          SET i 2     0062
0404 0017          17          0017
0405 0020          SET i 3     0063
0406 0021          2017        2017    Save 350 registers of quarter 0
0407 0022          SET i 4     0064    in quarter 4
0410 0023          -350        7427
0411 0024    #2A   LDA i 2     1022
0412 0025          STA i 3     1063
0413 0026          XSK i 4     0224
0414 0027          JMP 2A      6411
0415 0030    #2N   LDA i       1020
0416 0031          JMP 3A      6560    Set up storage and jump
0417 0032          STC 4B      4521    instructions
0420 0033          LDA i       1020
0421 0034          3A          0560
0422 0035          STA         1040
0423 0036          2E          0454
0424 0037          ADA i       1120
0425 0040          1           0001
0426 0041          STC 2F      4460
0427 0042    #2H   SET i 2     0062
0430 0043          3A-1        0557
0431 0044          SET i 3     0063
0432 0045          -1777+3A    6560    Clear memory from 3A to 1777
0433 0046          CLR         0011
0434 0047    #2B   STA i 2     1062
0435 0050          XSK i 3     0223
0436 0051          JMP 2B      6434
0437 0052          SET i 2     0062
0440 0053          3           0003
0441 0054          SET i 3     0063    Clear memory from 4 to 377
0442 0055          -372        7405
0443 0056          CLR         0011
0444 0057    #2D   STA i 2     1062
0445 0060          XSK i 3     0223
0446 0061          JMP 2D      6444
0447 0062    #2G   SET i 2     0062
0450 0063          -4          7773
0451 0064          LDA         1000
0452 0065          4A          0520
0453 0066          STA         1040
0454 0067    #2E   3A          0560    Test from 3A to 1777
0455 0070          LDA         1000
0456 0071          4B          0521
0457 0072          STA         1040
0460 0073    #2F   3A+1        0561
0461 0074          STA         1040
0462 0075          2C          0463
0463 0076    #2C   JMP 3A      6560
0464 0077    #1C   LDA         1000
```

```
0465  0100          2E                  0454  [JMPUP
0466  0101          ADA i               1120
0467  0102          6001                6001
0470  0103          SAE                 1440
0471  0104          0                   0000
0472  0105          HLT                 0000  Wrong JMP instruction in
0473  0106          XSK i 2             0222  register 0
0474  0107          JMP 0               6000
0475  0110          LDA                 1000
0476  0111          2E                  0454
0477  0112          SAE i               1460
0500  0113    #2K   1776                1776
0501  0114          JMP P+2             6503
0502  0115    #2L   JMP 2J              6522  To test 3 to 377
0503  0116          ADA i               1120
0504  0117          1                   0001
0505  0120          STA                 1040
0506  0121          2E                  0454
0507  0122          ADA i               1120  ]
0510  0123          1                   0001  ]  Increment JMP to next address
0511  0124          STC 2F              4460  ]
0512  0125          LDA                 1000  ]
0513  0126          2E                  0454  ]
0514  0127          ADA i               1120  ]
0515  0130          6000                6000  ]
0516  0131          STC 4B              4521  ]
0517  0132          JMP 2H              6427  ]
0520  0133    #4A   JMP 1C              6464
0521  0134    #4B   0                   0000  Current jump
0522  0135    #2J   LDA i               1020  ]
0523  0136          JMP 3               6003  ]
0524  0137          STC 4B              4521  ]
0525  0140          LDA i               1020  ]
0526  0141          3                   0003  ]
0527  0142          STA                 1040  ]
0530  0143          2E                  0454  ]
0531  0144          ADA i               1120  ]
0532  0145          1                   0001  ]  Test from 3 to 377
0533  0146          STC 2F              4460  ]
0534  0147          LDA i               1020  ]
0535  0150          376                 0376  ]
0536  0151          STC 2K              4500  ]
0537  0152          LDA i               1020  ]
0540  0153          JMP 2M              6543  ]
0541  0154          STC 2L              4502  ]
0542  0155          JMP 2H              6427  ]
0543  0156    #2M   XSK i 1             0221  Do once
0544  0157          JMP 2N              6415
0545  0160          SET i 2             0062  ]
0546  0161          17                  0017  ]
0547  0162          SET i 3             0063  ]
0550  0163          2017                2017  ]  Return control program to
0551  0164          SET i 4             0064  ]  quarter 0
0552  0165          -350                7427  ]
0553  0166    #2P   LDA i 3             1023  ]
0554  0167          STA i 2             1062  ]
0555  0170          XSK i 4             0224  ]
0556  0171          JMP 2P              6553  ]
0557  0172          JMP 34              6034  To contrl
0560  0173    #3A                       0000
```

```
0001    [JMPDWN
0002    [JUMP TEST
0003    [ TWO
0004    [CHECKS
0005    [REGISTERS
0006    [FROM 3A TO
0007    [ 1777 AND
0010    [FROM 3 TO
0011    [577
0012    ⊟400
0400 0013       63              0063    Test number
0401 0014       SET i 1         0061
0402 0015       7776            7776    Do once
0403 0016       JMP 600         6600
        0017    ⊟600
0600 0020       SET i 2         0062
0601 0021       17              0017
0602 0022       SET i 3         0063
0603 0023       2017            2017    Save 350 registers of quarter 0
0604 0024       SET i 4         0064    in quarter 4
0605 0025       -350            7427
0606 0026   #2A LDA i 2         1022
0607 0027       STA i 3         1063
0610 0030       XSK i 4         0224
0611 0031       JMP 2A          6606
0612 0032   #2N LDA i           1020
0613 0033       JMP 3A          6755
0614 0034       STC 4B          4716
0615 0035       LDA i           1020    Set up storage and jump
0616 0036       3A              0755    instructions
0617 0037       STA             1040
0620 0040       2E              0651
0621 0041       ADA i           1120
0622 0042       1               0001
0623 0043       STC 2F          4655
0624 0044   #2H SET i 2         0062
0625 0045       3A-1            0754
0626 0046       SET i 3         0063    Clear memory from 3A to 1777
0627 0047       -1777+3A        6755
0630 0050       CLR             0011
0631 0051   #2B STA i 2         1062
0632 0052       XSK i 3         0223
0633 0053       JMP 2B          6631
0634 0054       SET i 2         0062
0635 0055       3               0003
0636 0056       SET i 3         0063
0637 0057       -572            7205
0640 0060       CLR             0011    Clear memory from 4 to 577
0641 0061   #2D STA i 2         1062
0642 0062       XSK i 3         0223
0643 0063       JMP 2D          6641
0644 0064   #2G SET i 2         0062
0645 0065       -4              7773
0646 0066       LDA             1000
0647 0067       4A              0715
0650 0070       STA             1040
0651 0071   #2E 3A              0755    Test from 3A to 1777
0652 0072       LDA             1000
0653 0073       4B              0716
0654 0074       STA             1040
0655 0075   #2F 3A+1            0756
0656 0076       STA             1040
0657 0077       2C              0660
```

```
0660  0100      #2C JMP 3A          6755
0661  0101      #1C LDA             1000
0662  0102          2E              0651
0663  0103          ADA i           1120
0664  0104          6001            6001
0665  0105          SAE             1440
0666  0106          0               0000
0667  0107          HLT             0000    Wrong JMP instruction in
0670  0110          XSK i 2         0222    register 0
0671  0111          JMP 0           6000
0672  0112          LDA             1000
0673  0113          2E              0651
0674  0114          SAE i           1460
0675  0115      #2K 1776            1776
0676  0116          JMP *+2         6700
0677  0117      #2L JMP 2J          6717    To test 3 to 577
0700  0120          ADA i           1120
0701  0121          1               0001
0702  0122          STA             1040
0703  0123          2E              0651
0704  0124          ADA i           1120
0705  0125          1               0001    Increment JMP to next address
0706  0126          STC 2F          4655
0707  0127          LDA             1000
0710  0130          2E              0651
0711  0131          ADA i           1120
0712  0132          6000            6000
0713  0133          STC 4B          4716
0714  0134          JMP 2H          6624
0715  0135      #4A JMP 1C          6661
0716  0136      #4B 0               0000    Current jump
0717  0137      #2J LDA i           1020
0720  0140          JMP 3           6003
0721  0141          STC 4B          4716
0722  0142          LDA i           1020
0723  0143          3               0003
0724  0144          STA             1040
0725  0145          2E              0651
0726  0146          ADA i           1120    Test from 3 to 577
0727  0147          1               0001
0730  0150          STC 2F          4655
0731  0151          LDA i           1020
0732  0152          576             0576
0733  0153          STC 2K          4675
0734  0154          LDA i           1020
0735  0155          JMP 2M          6740
0736  0156          STC 2L          4677
0737  0157          JMP 2H          6624
0740  0160      #2M XSK i 1         0221    Do once
0741  0161          JMP 2N          6612
0742  0162          SET i 2         0062
0743  0163          17              0017
0744  0164          SET i 3         0063
0745  0165          2017            2017
0746  0166          SET i 4         0064    Return control program to
0747  0167          -350            7427    quarter 0
0750  0170      #2P LDA i 3         1023
0751  0171          STA i 2         1062
0752  0172          XSK i 4         0224
0753  0173          JMP 2P          6750
0754  0174          JMP 34          6034    To CONTRL
0755  0175      #3A                 0000
```

```
                0001    [TAPETS
                0002    @400
0400            0003            64              0064
0401            0004            LDA i           1020
0402            0005            11              0011
0403            0006            STC 46          4046
0404            0007            ADD 21          2021
0405            0010            STA i           1060
0406            0011    #1U                     0000
0407            0012            ADA i           1120
0410            0013            6001            6001
0411            0014            STA             1040
0412            0015            1A              0426
0413            0016            STA             1040
0414            0017            1M              0435
0415            0020            STA             1040
0416            0021            1N              0440
0417            0022            STA             1040
0420            0023            1O              0443
0421            0024            STA             1040
0422            0025            1Q              0447
0423            0026            STC 1B          4431
0424            0027            JMP 1F          6705
0425            0030            WCG i           0725  - Write a test pattern
0426            0031    #1A                     0000
0427            0032            JMP 1G          6722
0430            0033            RCG i           0721  - Read back the test pattern
0431            0034    #1B                     0000
0432            0035            JMP 1P          6735  - Test the test pattern
0433            0036            JMP 1G          6722
0434            0037            WCG i           0725
0435            0040    #1M                     0000
0436            0041            JMP 1F          6705
0437            0042            WCG             0705
0440            0043    #1N                     0000
0441            0044            JMP 1G          6722
0442            0045            RCG             0701
0443            0046    #1O                     0000
0444            0047            JMP 1P          6735
0445            0050            JMP 1G          6722
0446            0051            WCG             0705
0447            0052    #1Q                     0000
0450            0053            JMP 1F          6705
0451            0054            LDA             1000
0452            0055            1U              0406
0453            0056            ADD 1Y          2734
0454            0057            STA             1040
0455            0060            1U              0406
0456            0061    #2C     STA             1040
0457            0062            1R              0464
0460            0063            JMP 1S          6650
0461            0064            SET i 1         0061
0462            0065            -6              7771
0463            0066            WRI i           0726
0464            0067    #1R                     0000
0465            0070            SAE             1440
0466            0071            1V              0666
0467            0072            HLT             0000  - Wrong checksum in accumulator
0470            0073            LDA             1000
0471            0074            1R              0464
0472            0075            ADD 1Y          2734
0473            0076            STA             1040
0474            0077            1R              0464
```

```
0475  0100          JMP 1S          6650
0476  0101          XSK i 1         0221
0477  0102          JMP 1R-1        6463
0500  0103          JMP P+2         6502
0501  0104    #1X   HLT             0000 - Wrong transfer check from
0502  0105          SET i 1         0061   RDE instruction.
0503  0106          -6              7771
0504  0107          LDA             1000   Raise resume lever to try
0505  0110          1U              0406   again.
0506  0111          STC 1W          4510
0507  0112          RDE i           0722
0510  0113    #1W                   0000
0511  0114          SAE i           1460
0512  0115          7777            7777
0513  0116          JMP 1X          6501
0514  0117          LDA             1000
0515  0120          1W              0510
0516  0121          ADD 1Y          2734
0517  0122          STC 1W          4510
0520  0123          XSK i 1         0221
0521  0124          JMP 1W-1        6507
0522  0125    #2A   JMP 1P          6735
0523  0126          JMP 1G          6722
0524  0127          LDA i           1020
0525  0130          WRI             0706
0526  0131          STC 1R-1        4463
0527  0132          ADD 1Z          2703
0530  0133          STC 1W-1        4507
0531  0134          LDA i           1020
0532  0135          JMP 2B          6537
0533  0136          STC 2A          4522
0534  0137          LDA             1000
0535  0140          1U              0406
0536  0141          JMP 2C          6456
0537  0142    #2B   CLR             0011
0540  0143          STC 1C          4721
0541  0144          JMP 1P          6735
0542  0145          LDA i           1020
0543  0146          11              0011
0544  0147          STC 1C          4721
0545  0150          JMP 1F          6705
0546  0151          LDA             1000
0547  0152          1U              0406
0550  0153    #2I   STA             1040
0551  0154          2E              0571
0552  0155          STC 2D          4556
0553  0156          SET i 1         0061
0554  0157          -2              7775
0555  0160          WRC i           0724
0556  0161    #2D                   0000
0557  0162          LDA             1000
0560  0163          2D              0556
0561  0164          ADD 1Y          2734
0562  0165          STC 2D          4556
0563  0166          XSK i 1         0221
0564  0167          JMP 2D-1        6555
0565  0170          JMP 1G          6722
0566  0171          SET i 1         0061
0567  0172          -2              7775
0570  0173          RDC i           0720
0571  0174    #2E                   0000
0572  0175          LDA             1000
0573  0176          2E              0571
0574  0177          ADD 1Y          2734
```

```
0575  0200          STC 2E          4571
0576  0201          XSK i 1         0221
0577  0202          JMP 2E-1        6570
0600  0203          SET i 7         0067
0601  0204          JMP 2F          6607
0602  0205          SET i 3         0063
0603  0206          777             0777
0604  0207          SET i 4         0064
0605  0210          -1000           6777
0606  0211          JMP 1K          6745
0607  0212    #2F   JMP 1G          6722
0610  0213          LDA i           1020
0611  0214          WRC             0704
0612  0215          STC 2D-1        4555
0613  0216          ADD 2G          2704
0614  0217          STC 2E-1        4570
0615  0220          LDA i           1020
0616  0221          JMP 2H          6623
0617  0222          STC 2F-1        4606
0620  0223          LDA             1000
0621  0224          1U              0406
0622  0225          JMP 2I          6550
0623  0226    #2H   CLR             0011
0624  0227          STC 1C          4721
0625  0230          SET i 7         0067
0626  0231          JMP 2J          6630
0627  0232          JMP 1K          6745
0630  0233    #2J   JMP 1G          6722
0631  0234          LDA             1000
0632  0235          21              0021
0633  0236          ADD 1Y          2734
0634  0237          STC 2K          4640
0635  0240          SET i 1         0061
0636  0241          -10             7767
0637  0242          WRC i           0724
0640  0243    #2K                   0000
0641  0244          LDA             1000
0642  0245          2K              0640
0643  0246          ADD 2L          2765
0644  0247          STC 2K          4640
0645  0250          XSK i 1         0221
0646  0251          JMP 2K-1        6637
0647  0252          JMP 34          6034
      0253    [FORM A
      0254    [CHECKSUM
0650  0255    #1S   SET 7           0047
0651  0256          0               0000
0652  0257          SET i 4         0064
0653  0260          -400            7377
0654  0261          BCL i           1560
0655  0262          0777            0777
0656  0263          ROR 11          0311
0657  0264          MUL i           1260
0660  0265          400             0400
0661  0266          STC 17          4017
0662  0267          STC 1V          4666
0663  0270          CLR             0011
0664  0271          LDA 17          1017
0665  0272          LAM i           1220  - Two's complement addition
0666  0273    #1V                   0000
0667  0274          CLR             0011
0670  0275          LDA i 17        1037
0671  0276          XSK i 4         0224
0672  0277          JMP 1V-1        6665
```

```
0673  0300          LDA                 1000  [TAPETS
0674  0301          1V                  0666
0675  0302          COM                 0017
0676  0303          STC 1V              4666
0677  0304          ADD 2L              2765
0700  0305          LAM                 1200
0701  0306          1V                  0666
0702  0307          JMP 7               6007
0703  0310    #1Z   RDE                 0702
0704  0311    #2G   RDC                 0700
      0312    [GENERATE TEST
      0313    [PATTERN IN
      0314    [ON 2 3 4 5 6 7
0705  0315    #1F   SET 7               0047
0706  0316          0                   0000
0707  0317          JMP 1L              6753      The test pattern
0710  0320    #1D   ADD 1C              2721      is a count by 11.
0711  0321          STA i 1             1061
0712  0322          XSK i 2             0222
0713  0323          JMP 1D              6710
0714  0324    #1E   ADD 1C              2721
0715  0325          STA i 3             1063
0716  0326          XSK i 4             0224
0717  0327          JMP 1E              6714
0720  0330          JMP 7               6007
0721  0331    #1C   11                  0011
      0332    [CLEAR OUT
      0333    [ON 2 3 4 5 6 7
0722  0334    #1GSET 7                  0047
0723  0335          0                   0000
0724  0336          JMP 1L              6753
0725  0337    #1H   STA i 1             1061
0726  0340          XSK i 2             0222
0727  0341          JMP 1H              6725
0730  0342    #1I   STA i 3             1063
0731  0343          XSK i 4             0224
0732  0344          JMP 1I              6730
0733  0345          JMP 7               6007
0734  0346    #1Y   1001                1001
      0347    [TEST THE TEST
      0350    [PATTERN READ
      0351    [BACK FROM TAPE
0735  0352    #1P   SET 7               0047
0736  0353          0                   0000
0737  0354          JMP 1L              6753
0740  0355    #1J   ADD 1C              2721
0741  0356          SAE i 1             1461
0742  0357          HLT                 0000  - Error in test pattern.
0743  0360          XSK i 2             0222    Beta register 7 indicates
0744  0361          JMP 1J              6740    the vicinity in program
0745  0362    #1K   ADD 1C              2721    where a tape instruction
0746  0363          SAE i 3             1463    failed.
0747  0364          HLT                 0000
0750  0365          XSK i 4             0224
0751  0366          JMP 1K              6745
0752  0367          JMP 7               6007
0753  0370    #1L   SET i 1             0061
0754  0371          777                 0777
0755  0372          SET i 2             0062
0756  0373          -1000               6777
0757  0374          SET i 3             0063
0760  0375          3777                3777
0761  0376          SET i 4             0064
0762  0377          -2000               5777
```

```
0763    0400          CLR             0011    [TAPETS
0764    0401          JMP 0           6000
0765    0402    #2L   1               0001
```

```
                0001    [MTBTST
                0002    ⊟400
0400            0003        65              0065
0401            0004        MTB i           0723
0402            0005        10              0010
0403            0006    #1A IBZ             0453 - If tape runs off end here,
0404            0007        JMP P-1         6403   there is trouble with IBZ
0405            0010        MTB i           0723   or MTB.
0406            0011        10              0010
0407            0012        APO i           0471
0410            0013        COM             0017
0411            0014        ADA i           1120
0412            0015        2               0002
0413            0016        APO             0451
0414            0017        JMP 1A          6403
0415            0020        MTB i           0723 - Near Block 10
0416            0021        700             0700
0417            0022        SET i 1         0061
0420            0023        -1032           6745
0421            0024    #1B SET i 2         0062
0422            0025        0               0000
0423            0026        XSK i 2         0222   Long delay to get tape
0424            0027        JMP P-1         6423       to Block 640
0425            0030        XSK i 1         0221
0426            0031        JMP 1B          6421
0427            0032        MTB             0703
0430            0033        700             0700 - Stop tape
0431            0034        APO i           0471
0432            0035        COM             0017
0433            0036        ADA i           1120   Is tape above Block 600?
0434            0037        100             0100
0435            0040        APO             0451
0436            0041        HLT             0000 -  Tape either stopped when
0437            0042        MTB i           0723    i bit was on, or tape
0440            0043        100             0100    motion was too slow.
0441            0044        SET i 1         0061
0442            0045        -703            7074
0443            0046    #1C SET i 2         0062
0444            0047        0               0000
0445            0050        XSK i 2         0222   Long delay to get tape
0446            0051        JMP P-1         6445       to Block 100
0447            0052        XSK i 1         0221
0450            0053        JMP 1C          6443
0451            0054        MTB             0703
0452            0055        100             0100 - Stop tape
0453            0056        APO i           0471
0454            0057        COM             0017
0455            0060        ADA i           1120
0456            0061        100             0100
0457            0062        APO             0451
0460            0063        HLT             0000 - Tape probably stopped
0461            0064        JMP 34          6034   when i bit was on.
```

```
                0001    [DISTST
                0002    @400
0400            0003        66                  0066
0401            0004        SET i 15            0075
0402            0005        -100                7677
0403            0006    #1D SET i 1             0061
0404            0007        0                   0000
0405            0010    #1E CLR                 0011
0406            0011        STC 1A              4416
0407            0012        STC 1B              4422
0410            0013        STC 1C              4425
0411            0014        STC 2A              4435
0412            0015        STC 2B              4441
0413            0016        LDA i               1020
0414            0017    #1F 1                   0001
0415            0020        STA i               1060
0416            0021    #1A                     0000
0417            0022        MUL                 1240
0420            0023        4000+P-2            4416
0421            0024        STA i               1060
0422            0025    #1B                     0000
0423            0026        MSC 5               0005
0424            0027        STA i               1060
0425            0030    #1C                     0000
0426            0031    #2C LDA i 1             1021
0427            0032        LDA                 1000
0430            0033        1                   0001
0431            0034        MUL                 1240
0432            0035        4001                4001
0433            0036        COM                 0017
0434            0037        STA i               1060
0435            0040    #2A                     0000
0436            0041        MSC 5               0005
0437            0042        COM                 0017
0440            0043        STA i               1060
0441            0044    #2B                     0000
0442            0045        ADD 1C              2425
0443            0046        STC 3A              4505
0444            0047        ADD 2A              2435
0445            0050        ADD 1B              2422
0446            0051        STC 3F              4511
0447            0052        LDA i               1020
0450            0053        1                   0001
0451            0054        STC 3B              4506
0452            0055        JMP P+2             6454
0453            0056    #3D STC 3A              4505
0454            0057        ADD 3C              2507
0455            0060        ADM                 1140
0456            0061        3B                  0506
0457            0062        ADD 3A              2505
0460            0063        AZE                 0450
0461            0064        APO i               0471
0462            0065        JMP 3D              6453
0463            0066    #3J ADD 3E              2510
0464            0067        STC 3A              4505
0465            0070        ADD 3F              2511
0466            0071        APO i               0471
0467            0072        JMP P+2             6471
0470            0073        JMP 3K              6500
0471            0074        ADD 3G              2512
0472            0075        STC 3F              4511
0473            0076        ADD 3A              2505
0474            0077        ADD 3H              2513
```

```
0475  0100          APO i              0471
0476  0101          JMP 3D             6453
0477  0102          JMP 3J             6463
0500  0103    #3K   LDA                1000
0501  0104          3B                 0506
0502  0105          COM                0017
0503  0106          SCR 1              0341
0504  0107          JMP 4A             6514
0505  0110    #3A                      0000
0506  0111    #3B                      0000
0507  0112    #3C   -2                 7775
0510  0113    #3E   1                  0001
0511  0114    #3F                      0000
0512  0115    #3G   -1                 7776
0513  0116    #3H   3777               3777
0514  0117    #4A   STC 4B             4603
0515  0120          ADD 1              2001
0516  0121          ADD 4C             2604
0517  0122          STC 2              4002
0520  0123          ADD 1              2001
0521  0124          ADD 4C             2604
0522  0125          STC 2              4002
0523  0126          ADD 1              2001
0524  0127          COM                0017
0525  0130          ADD 4C             2604
0526  0131          STC 3              4003
0527  0132          ADD 4B             2603
0530  0133          DIS 2              0142
0531  0134          DIS 3              0143
0532  0135          COM                0017
0533  0136          DIS 2              0142
0534  0137          DIS 3              0143
0535  0140          CLR                0011
0536  0141          ADD 1              2001
0537  0142          COM                0017
0540  0143          ADD 1A             2416
0541  0144          AZE                0450
0542  0145          JMP 1E             6405
0543  0146          LDA                1000
0544  0147          1F                 0414
0545  0150          ADA i              1120
0546  0151          1                  0001
0547  0152          STC 1F             4414
0550  0153          XSK i 15           0235
0551  0154          JMP 1D             6403
0552  0155    #1J   SET i 16           0076
0553  0156          1764               1764
0554  0157    #1H   SET i 13           0073
0555  0160          377                0377
0556  0161          SET i 14           0074
0557  0162          -377               7400
0560  0163          SET i 15           0075
0561  0164          -777               7000
0562  0165          SET i 1            0061
0563  0166          0                  0000
0564  0167    #1I   LDA i              1020
0565  0170          -1                 7776
0566  0171          ADM                1140
0567  0172          13                 0013
0570  0173          DIS i 1            0161
0571  0174          LDA i              1020
0572  0175          1                  0001
0573  0176          ADM                1140
0574  0177          14                 0014
```

```
0575    0200          DIS 1           0141    [DISTST
0576    0201          XSK i 15        0235
0577    0202          JMP 1I          6564
0600    0203          XSK i 16        0236
0601    0204          JMP 1H          6554
0602    0205          JMP 34          6034
0603    0206    #4B                   0000
0604    0207    #4C 377               0377
```

```
                0001    [DSCTST
                0002    ⊟400
0400            0003        67              0067
0401            0004    #1G SET i 17        0077
0402            0005        1700            1700
0403            0006    #1C SET i 1         0061
0404            0007        300             0300
0405            0010        SET i 2         0062
0406            0011        -7              7770
0407            0012        SET i 3         0063
0410            0013        1A-1            0455
0411            0014    #1B CLR             0011
0412            0015        DSC i 3         1763
0413            0016        XSK i 3         0223
0414            0017        DSC 3           1743
0415            0020        LDA i           1020
0416            0021        4               0004
0417            0022        ADM             1140
0420            0023        1               0001
0421            0024        XSK i 2         0222
0422            0025        JMP 1B          6411
0423            0026        SET i 1         0061
0424            0027        0               0000
0425            0030        SET i 2         0062
0426            0031        -100            7677
0427            0032    #1E LDA i           1020
0430            0033        200             0200
0431            0034        DSC i           1760
0432            0035        7777            7777
0433            0036        DSC i           1760
0434            0037        7777            7777
0435            0040        XSK i 2         0222
0436            0041        JMP 1E          6427
0437            0042        SET i 1         0061
0440            0043        0               0000
0441            0044        SET i 2         0062
0442            0045        -100            7677
0443            0046    #1F LDA  i          1020
0444            0047        -200            7577
0445            0050        DSC             1740
0446            0051        1D              0474
0447            0052        DSC             1740
0450            0053        1D+1            0475
0451            0054        XSK i 2         0222
0452            0055        JMP 1F          6443
0453            0056        XSK i 17        0237
0454            0057        JMP 1C          6403
0455            0060        JMP 34          6034
0456            0061    #1A 4177            4177
0457            0062        3641            3641
0460            0063        7741            7741
0461            0064        0041            0041
0462            0065        5121            5121
0463            0066        4651            4651
0464            0067        4477            4477
0465            0070        3044            3044
0466            0071        0177            0177
0467            0072        0301            0301
0470            0073        4477            4477
0471            0074        7744            7744
0472            0075        0770            0770
0473            0076        7007            7007
0474            0077    #1D 7777            7777
```

```
         0001     [OVFT1
          0002     [OVERFLOW
          0003     [TEST ONE
          0004     [OVF IS SKP14
          0005     ⊟400
0400      0006          700              0700
0401      0007          SET i 1          0061
0402      0010          7776             7776
          0011     [POSITIVE
          0012     [NUMBERS
          0013     [WITH OVF
0403      0014     #5A SET i 2           0062
0404      0015          3A-1             0620
0405      0016          SET i 3          0063
0406      0017          -3               7774
0407      0020          LDA i 2          1022
0410      0021          STC 1A           4415
0411      0022     #4A LDA i             1020
0412      0023          0                0000
0413      0024          STC 3B           4424
0414      0025     #2A LDA i             1020
0415      0026     #1A 0                 0000     Positive pattern.
0416      0027          ADD 3B           2424
0417      0030          SKP 14           0454
0420      0031          JMP 1B           6425
0421      0032          APO i            0471
0422      0033          HLT              0000     OVF indication, but
0423      0034          JMP 1B+2         6427     no overflow occurred.
0424      0035     #3B                   0000     Number added to current
0425      0036     #1B APO               0451     accumulator value.
0426      0037          HLT              0000     No OVF indication, but
0427      0040          LDA              1000     overflow occurred.
0430      0041          3B               0424
0431      0042          SAE i            1460
0432      0043          3777             3777
0433      0044          JMP 1C           6442
0434      0045          XSK i 3          0223
0435      0046          JMP P+2          6437
0436      0047          JMP 1D           6446
0437      0050          LDA i 2          1022     Put new positive
0440      0051          STC 1A           4415     pattern into 1A.
0441      0052          JMP 4A           6411
0442      0053     #1C ADA i             1120     Increment counter in 3B.
0443      0054          1                0001
0444      0055          STC 3B           4424
0445      0056          JMP 2A           6414
          0057     [POSITIVE
          0060     [NUMBERS
          0061     [WITH OVF i
0446      0062     #1D SET i 2           0062
0447      0063          3A-1             0620
0450      0064          SET i 3          0063
0451      0065          -3               7774
0452      0066          LDA i 2          1022
0453      0067          STC 1E           4460
0454      0070     #4B LDA i             1020
0455      0071          0                0000
0456      0072          STC 3B           4424
0457      0073     #2B LDA i             1020
0460      0074     #1E 0                 0000     Positive pattern
0461      0075          ADD 3B           2424
0462      0076          SKP i 14         0474
0463      0077          JMP P+2          6465
```

```
0464  0100          JMP 1F          6470  [OVFT1
0465  0101          APO i           0471
0466  0102          HLT             0000 — OVF indicated, but
0467  0103          JMP 1F+2        6472   no overflow.
0470  0104    #1F   APO             0451
0471  0105          HLT             0000 — No OVF indicated,
0472  0106          LDA             1000   but overflow occurred.
0473  0107          3B              0424
0474  0110          SAE i           1460
0475  0111          3777            3777
0476  0112          JMP 1G          6505
0477  0113          XSK i 3         0223
0500  0114          JMP *+2         6502
0501  0115          JMP 1H          6511
0502  0116          LDA i 2         1022
0503  0117          STC 1E          4460
0504  0120          JMP 4B          6454
0505  0121    #1G   ADA i           1120
0506  0122          1               0001
0507  0123          STC 3B          4424
0510  0124          JMP 2B          6457
      0125    [NEGATIVE
      0126    [NUMBERS
      0127    [WITH OVF
0511  0130    #1H   SET i 2         0062
0512  0131          3C-1            0623
0513  0132          SET i 3         0063
0514  0133          -3              7774
0515  0134          LDA i 2         1022
0516  0135          STC 1J          4523
0517  0136    #4C   LDA i           1020
0520  0137          4000            4000
0521  0140          STC 3B          4424
0522  0141    #2C   LDA i           1020
0523  0142    #1J   0               0000   Negative pattern.
0524  0143          ADD 3B          2424
0525  0144          SKP 14          0454
0526  0145          JMP 1K          6532
0527  0146          APO             0451
0530  0147          HLT             0000 — OVF indicated,but
0531  0150          JMP 1K+2        6534   no overflow.
0532  0151    #1K   APO i           0471
0533  0152          HLT             0000 — No OVF indicated,
0534  0153          LDA             1000   but overflow occurred.
0535  0154          3B              0424
0536  0155          SAE i           1460
0537  0156          7777            7777
0540  0157          JMP 1L          6547
0541  0160          XSK i 3         0223
0542  0161          JMP *+2         6544
0543  0162          JMP 1M          6553
0544  0163          LDA i 2         1022
0545  0164          STC 1J          4523
0546  0165          JMP 4C          6517
0547  0166    #1L   ADA i           1120
0550  0167          1               0001
0551  0170          STC 3B          4424
0552  0171          JMP 2C          6522
      0172    [NEGATIVE
      0173    [NUMBERS
      0174    [WITH OVF i
0553  0175    #1M   SET i 2         0062
0554  0176          3C-1            0623
0555  0177          SET i 3         0063
```

```
0556  0200          -3                7774
0557  0201          LDA i 2           1022
0560  0202          STC 1N            4565
0561  0203  #4D     LDA i             1020
0562  0204          4000              4000
0563  0205          STC 3B            4424
0564  0206  #2D     LDA i             1020
0565  0207  #1N     0                 0000  - Negative pattern
0566  0210          ADD 3B            2424
0567  0211          SKP i 14          0474
0570  0212          JMP P+2           6572
0571  0213          JMP 1P            6575
0572  0214          APO               0451
0573  0215          HLT               0000  - Overflow indicated,
0574  0216          JMP 1P+2          6577        but none occurred
0575  0217  #1P     APO i             0471
0576  0220          HLT               0000  - No OVF indicated,
0577  0221          LDA               1000        but overflow occurred.
0600  0222          3B                0424
0601  0223          SAE i             1460
0602  0224          7777              7777
0603  0225          JMP 1R            6612
0604  0226          XSK i 3           0223
0605  0227          JMP P+2           6607
0606  0230          JMP 1S            6616
0607  0231          LDA i 2           1022
0610  0232          STC 1N            4565
0611  0233          JMP 4D            6561
0612  0234  #1R     ADA i             1120
0613  0235          1                 0001
0614  0236          STC 3B            4424
0615  0237          JMP 2D            6564
0616  0240  #1S     LDA i             1020
0617  0241          4000              4000
0620  0242          ADA i             1120
0621  0243          1000              1000
0622  0244          SKP i 14          0474
0623  0245          HLT               0000  - No possibility of OVF, but
0624  0246          XSK i 1           0221        overflow was indicated.
0625  0247          JMP 5A            6403
0626  0250          JMP 34            6034
0627  0251  #3A     1111              1111
0630  0252          2222              2222  - Positive number patterns
0631  0253          3333              3333
0632  0254  #3C     4444              4444
0633  0255          5555              5555  - Negative number patterns
0634  0256          6666              6666
```

```
                0001    [ZTA T1
                0002    [ZZZ=SKP 15
                0003    [ZTA=MSC 5
                0004    [ZTA AND ZZZ
                0005    [TEST ONE
                0006    ⊟400
0400            0007        701             0701
0401            0010        SET i 1         0061
0402            0011        7776            7776    Do once
0403            0012    #2D LDA i           1020 ┐
0404            0013        0               0000 │
0405            0014        STA             1040 │
0406            0015        1A              0411 │  Set up
0407            0016        STC 2A          4434 │
0410            0017        LDA i           1020 ┘
0411            0020    #1A 0               0000    Pattern to be moved
0412            0021        SCR 14          0354    A to Z
0413            0022        MSC 5           0005    Z to A
0414            0023        SAE             1440
0415            0024        2A              0434
0416            0025        HLT             0000    Improper Z to A transfer
0417            0026        LDA             1000
0420            0027        1A              0411
0421            0030        SAE i           1460
0422            0031        3777            3777    Finished ?
0423            0032        JMP P+2         6425
0424            0033        JMP 2B          6435
0425            0034        ADA i           1120 ┐
0426            0035        1               0001 │
0427            0036        STA             1040 │
0430            0037        1A              0411 │  Increment pattern
0431            0040        SCR 1           0341 │
0432            0041        STC 2A          4434 │
0433            0042        JMP 1A-1        6410 ┘
0434            0043    #2A                 0000    Correct pattern for A after ZTA
0435            0044    #2B LDA i           1020
0436            0045        0               0000
0437            0046        STC 1B          4441
0440            0047        LDA i           1020
0441            0050    #1B 0               0000    Pattern to be moved
0442            0051        SCR 14          0354    A to Z
0443            0052        MSC 5           0005    Z to A
0444            0053        ROL 1           0241
0445            0054        SKP i 15        0475    ZZZ i
0446            0055        JMP 1C          6451
0447            0056        ADA i           1120
0450            0057        1               0001
0451            0060    #1C SAE             1440
0452            0061        1B              0441
0453            0062        HLT             0000    ZZZ i not correct
0454            0063        LDA             1000    Pattern at 1B, error pattern
0455            0064        1B              0441    in accumulator
0456            0065        SAE i           1460
0457            0066        3777            3777
0460            0067        JMP P+2         6462
0461            0070        JMP 2C          6466
0462            0071        ADA i           1120
0463            0072        1               0001
0464            0073        STC 1B          4441
0465            0074        JMP 1B-1        6440
0466            0075    #2C LDA i           1020
0467            0076        0               0000
0470            0077        STC 1D          4472
```

```
0471  0100          LDA i          1020  [ZTA T1
0472  0101  #1D D    0              0000  Proper pattern for ZZZ
0473  0102          SCR 14         0354
0474  0103          MSC 5          0005
0475  0104          ROL 1          0241
0476  0105          SKP 15         0455  ZZZ
0477  0106          JMP P+2        6501
0500  0107          JMP 1E         6503
0501  0110          ADA i          1120
0502  0111          1              0001
0503  0112  #1E SAE                1440
0504  0113          1D             0472
0505  0114          HLT            0000  ZZZ not correct
0506  0115          LDA            1000  Error pattern in accumulator
0507  0116          1D             0472
0510  0117          SAE i          1460
0511  0120          3777           3777
0512  0121          JMP P+2        6514
0513  0122          JMP 1F         6520
0514  0123          ADA i          1120
0515  0124          1              0001
0516  0125          STC 1D         4472
0517  0126          JMP 1D-1       6471
0520  0127  #1F XSK i 1            0221
0521  0130          JMP 2D         6403
0522  0131          JMP 34         6034
```

```
                0001    [ZCLR1
                0002    [Z REGISTER
                0003    [SHOULD NOT
                0004    [BE DISTURBED
                0005    [BY MOST OF
                0006    [ORDER CODE
                0007    ⊟400
0400            0010        702             0702
0401            0011        SET i 1         0061
0402            0012        7776            7776
0403            0013    #1E SET i 2         0062
0404            0014        2A-1            0454
0405            0015        SET i 3         0063
0406            0016        -41             7736
0407            0017        SET i 4         0064
0410            0020        3A              0516
0411            0021        LDA i 2         1022
0412            0022        STC 1B          4421
0413            0023    #1D LDA i           1020
0414            0024        0               0000
0415            0025        STC 1A          4417
0416            0026        LDA i           1020
0417            0027    #1A 0               0000    Pattern in Z before test
0420            0030        SCR 14          0354    instruction is executed
0421            0031    #1B 0               0000    Current instruction
0422            0032        NOP             0016
0423            0033        NOP             0016
0424            0034        NOP             0016
0425            0035        MSC 5           0005
0426            0036        ROL 1           0241
0427            0037        SKP i 15        0475
0430            0040        JMP P+3         6433
0431            0041        ADA i           1120
0432            0042        1               0001
0433            0043        SAE             1440
0434            0044        1A              0417
0435            0045        HLT             0000    Z register changed by
0436            0046        SAE i           1460    instruction in 1B
0437            0047        3777            3777
0440            0050        JMP P+2         6442
0441            0051        JMP 1C          6446
0442            0052        ADA i           1120 ┐
0443            0053        1               0001 │  Put new pattern in Z
0444            0054        STC 1A          4417 │
0445            0055        JMP 1A-1        6416 ┘
0446            0056    #1C LDA i 2         1022 ┐
0447            0057        STC 1B          4421 │
0450            0060        XSK i 3         0223 │
0451            0061        JMP 1D          6413 │  Put new instruction in 1B
0452            0062        XSK i 1         0221 │
0453            0063        JMP 1E          6403 │
0454            0064        JMP 34          6034 ┘
0455            0065    #2A ADA             1100 ┐
0456            0066        ADD 1           2001 │
0457            0067        ADM 4           1144 │  Test instructions
0460            0070        APO             0451 │
0461            0071        ATR             0014 │
0462            0072        AZE             0450 │
0463            0073        BCL             1540 │
0464            0074        BCO             1640 │
0465            0075        BSE             1600 │
0466            0076        COM             0017 │
0467            0077        DIS             0140 │
```

```
0470  0100          JMP  1B+1          6422  [ZCLR1
0471  0101          KBD                0515
0472  0102          KST                0415
0473  0103          LAM  4             1204
0474  0104          LDA                1000
0475  0105          LDH                1300
0476  0106          LSW                0517
0477  0107          LZE                0452
0500  0110          OPR  1             0501
0501  0111          ROL  1             0241
0502  0112          RSW                0516
0503  0113          RTA                0015
0504  0114          SAE                1440
0505  0115          SET  i 5           0065
0506  0116          SHD                1400
0507  0117          SNS  0             0440
0510  0120          SRO  4             1504
0511  0121          STA  4             1044
0512  0122          STC  3A            4516
0513  0123          STH  4             1344
0514  0124          SXL                0400
0515  0125          XSK                0200
0516  0126    #3A                      0000  Garbage
```

```
                0001    [ZCLRT2
                0002    [SAM SHOULD
                0003    [CLEAR Z
                0004    [KNOB 0
                0005    [MUST BE
                0006    [FULLY
                0007    [CLOCKWISE
                0010    ⊟400
0400            0011        703             0703
0401            0012        SET i 1         0061
0402            0013        7770            7770
0403            0014    #1C LDA i           1020
0404            0015        0               0000
0405            0016        STC 1A          4407
0406            0017        LDA i           1020
0407            0020    #1A 0               0000    Pattern in Z before SAM
0410            0021        SCR 14          0354
0411            0022        SAM 0           0100    Should get 177
0412            0023        SAE i           1460
0413            0024        177             0177
0414            0025        HLT             0000    Either Z was not cleared properly
0415            0026        LDA             1000    or SAM0 did not see 177
0416            0027        1A              0407
0417            0030        SAE i           1460
0420            0031        7777            7777
0421            0032        JMP P+2         6423
0422            0033        JMP 1B          6427
0423            0034        ADA i           1120                Try knobs
0424            0035        1               0001
0425            0036        STC 1A          4407
0426            0037        JMP 1A-1        6406
0427            0040    #1B XSK i 1         0221
0430            0041        JMP 1C          6403
0431            0042        JMP 34          6034
```

```
      0001      [ENIT1
      0002      [ENI AND PIN
      0003      [TEST
      0004      [ENI IS MSC10
      0005      [PIN IS SKP 6
      0006      ⊟400
0400  0007           704              0704
0401  0010           SET i 17         0077   Do 7 times
0402  0011           7770             7770
0403  0012      #2A  SET i 1          0061
0404  0013           17               0017
0405  0014           SET i 2          0062
0406  0015           3777             3777
0407  0016           SET i 3          0063
0410  0017           -100             7677
0411  0020      #1A  LDA i 1          1021   Save CONTRL in QN 4
0412  0021           STA i 2          1062
0413  0022           XSK i 3          0223
0414  0023           JMP 1A           6411
0415  0024      #7B  CLR              0011
0416  0025           SET i 1          0061
0417  0026           0                0000
0420  0027           SET i 2          0062
0421  0030           -376             7401
0422  0031      #1B  STA i 1          1061
0423  0032           XSK i 2          0222
0424  0033           JMP 1B           6422
0425  0034           SET i 1          0061   Clear memory
0426  0035           7A               0546
0427  0036      #1C  STA i 1          1061
0430  0037           XSK 1            0201
0431  0040           JMP 1C           6427
0432  0041           LDA i            1020
0433  0042           JMP 1D           6531
0434  0043           STC 21           4021
0435  0044           MSC 10           0010
0436  0045           JMP P+2          6440
0437  0046           HLT              0000   Was interrupted after JMP
0440  0047           CLR              0011
0441  0050           SAE i            1460
0442  0051           1234             1234
0443  0052           HLT              0000   Did not interrupt after CLR
0444  0053           LDA i            1020
0445  0054           JMP 1E           6534
0446  0055           STC 21           4021
0447  0056           MSC 10           0010
0450  0057           NOP              0016
0451  0060           SAE i            1460
0452  0061           4321             4321
0453  0062           HLT              0000   Did not interrupt after NOP
0454  0063           LDA i            1020
0455  0064           JMP 1F           6545
0456  0065           STC 21           4021
0457  0066           MSC 10           0010
0460  0067           KBD i            0535
0461  0070           SKP 6            0446
0462  0071           HLT              0000   Pause was interrupted and
0463  0072           MSC 10           0010   PIN did not skip
0464  0073           KBD i            0535
0465  0074           SKP i 6          0466
0466  0075           JMP P+2          6470
0467  0076           HLT              0000   Pause was interrupted and
0470  0077           CHK              0707   PIN i skipped
```

```
0471  0100          70                0070
0472  0101          SKP 6             0446
0473  0102          JMP P+2           6475
0474  0103          HLT               0000  Pause was not interrupted and
0475  0104          CHK               0707  PIN skipped
0476  0105          72                0072
0477  0106          SKP i 6           0466
0500  0107          HLT               0000  Pause was not interrupted and
0501  0110          LDA i             1020  PIN i did not skip
0502  0111          OPR               0500
0503  0112          STC 21            4021
0504  0113          MSC 10            0010
0505  0114          NOP               0016
0506  0115          KBD i             0535
0507  0116          SKP 6             0446
0510  0117          HLT               0000  OPR instruction in register
0511  0120          LDA i             1020  21 turned off the ENFF
0512  0121          JMP 1F            6545
0513  0122          STC 21            4021  Turns off ENFF
0514  0123          XSK i 17          0237
0515  0124          JMP 7B            6415
0516  0125          SET i 1           0061
0517  0126          17                0017
0520  0127          SET i 2           0062
0521  0130          3777              3777
0522  0131          SET i 3           0063
0523  0132          -100              7677
0524  0133  #2B     LDA i 2           1022
0525  0134          STA i 1           1061
0526  0135          XSK i 3           0223
0527  0136          JMP 2B            6524
0530  0137          JMP 34            6034
0531  0140  #1D     LDA i             1020
0532  0141          1234              1234
0533  0142          JMP 0             6000
0534  0143  #1E     SET 1             0041
0535  0144          0                 0000
0536  0145          SET i 2           0062
0537  0146          1000              1000
0540  0147          XSK i 2           0222
0541  0150          JMP P-1           6540
0542  0151          LDA i             1020
0543  0152          4321              4321
0544  0153          JMP 1             6001
0545  0154  #1F     NOP               0016
0546  0155  #7A     JMP 0             6000
```

```
                0001    [MISCTS
                0002    [MISCELLANEOUS
                0003    [INSTRUCTIONS
                0004    [TEST
                0005    B400
0400    0006            71              0071
0401    0007            SNS 0           0440
0402    0010            HLT             0000
0403    0011            SNS 1           0441
0404    0012            HLT             0000
0405    0013            SNS 2           0442
0406    0014            HLT             0000
0407    0015            SNS 3           0443
0410    0016            HLT             0000
0411    0017            SNS 4           0444
0412    0020            HLT             0000
0413    0021            SNS 5           0445
0414    0022            HLT             0000
0415    0023            SNS i 0         0460
0416    0024            JMP P+2         6420
0417    0025            HLT             0000
0420    0026            SNS i 1         0461
0421    0027            JMP P+2         6423
0422    0030            HLT             0000
0423    0031            SNS i 3         0463
0424    0032            JMP P+2         6426
0425    0033            HLT             0000
0426    0034            SNS i 4         0464
0427    0035            JMP P+2         6431
0430    0036            HLT             0000
0431    0037            SNS i 5         0465
0432    0040            JMP P+2         6434
0433    0041            HLT             0000
0434    0042            RSW             0516
0435    0043            SAE i           1460
0436    0044            300             0300
0437    0045            HLT             0000
0440    0046            LSW             0517
0441    0047            SAE i           1460
0442    0050            700             0700
0443    0051            HLT             0000
0444    0052            SXL 0           0400
0445    0053            HLT             0000
0446    0054            SXL 1           0401
0447    0055            HLT             0000
0450    0056            SXL 2           0402
0451    0057            HLT             0000
0452    0060            SXL 3           0403
0453    0061            HLT             0000
0454    0062            SXL 4           0404
0455    0063            HLT             0000
0456    0064            SXL 5           0405
0457    0065            HLT             0000
0460    0066            SXL 6           0406
0461    0067            HLT             0000
0462    0070            SXL 7           0407
0463    0071            HLT             0000
0464    0072            SXL 10          0410
0465    0073            HLT             0000
0466    0074            SXL 11          0411
0467    0075            HLT             0000
0470    0076            SXL 12          0412
0471    0077            HLT             0000
```

If machine halts,

either the sense

switches do not show

a 77, or a sense

switch instruction

is failing.

- Wrong number seen in right switches

- Wrong number seen in left switches

- A disconnected external level line should always be negative.

  A ground level will cause a halt.

```
0472  0100  SXL 13          0413
0473  0101  HLT             0000
0474  0102  SXL i 0         0420
0475  0103  JMP P+2         6477
0476  0104  HLT             0000
0477  0105  SXL i 1         0421
0500  0106  JMP P+2         6502
0501  0107  HLT             0000
0502  0110  SXL i 2         0422
0503  0111  JMP P+2         6505
0504  0112  HLT             0000
0505  0113  SXL i 3         0423
0506  0114  JMP P+2         6510
0507  0115  HLT             0000
0510  0116  SXL i 4         0424
0511  0117  JMPP+2          6513
0512  0120  HLT             0000
0513  0121  SXL i 5         0425
0514  0122  JMPP+2          6516
0515  0123  HLT             0000
0516  0124  SXL i 6         0426
0517  0125  JMP P+2         6521
0520  0126  HLT             0000
0521  0127  SXL i 7         0427
0522  0130  JMP P+2         6524
0523  0131  HLT             0000
0524  0132  SXL i 10        0430
0525  0133  JMP P+2         6527
0526  0134  HLT             0000
0527  0135  SXL i 11        0431
0530  0136  JMP P+2         6532
0531  0137  HLT             0000
0532  0140  SXL i 12        0432
0533  0141  JMP P+2         6535
0534  0142  HLT             0000
0535  0143  SXL i 13        0433
0536  0144  JMP  P+2        6540
0537  0145  HLT             0000
0540  0146  KST i           0435
0541  0147  KBD             0515
0542  0150  KST i           0435
0543  0151  HLT             0000
0544  0152  KST             0415
0545  0153  JMP P+2         6547
0546  0154  HLT             0000
0547  0155  JMP 34          6034
```

KST always sees a key struck.

```
                0001    [GETLEP                         [GETLEP
                0002    [GET LPFROG
                0003    ■400
0400            0004        4002                4002    Program number
0401            0005    #2S JMP P+2             6403
0402            0006        0                   0000
0403            0007        LDA                 1000
0404            0010        1R+1                0021
0405            0011        BCL i               1560
0406            0012        1000                1000    Reads LPFROG Into QN 1
0407            0013        ADA i               1120
0410            0014        1                   0001
0411            0015        STC P+2             4413
0412            0016        RDC                 0700
0413            0017        0                   0000
0414            0020        JMP 20              6020
```

```
0001  0001        (LEAP FROG
      0002        @1
0001  0003            20                  0020   Start of present block
0002  0004            20                  0020   Start of next block
0003  0005            0                   0000   Counter and TEMP
0004  0006            0                   0000   Address in current block
0005  0007            0                   0000   Address in next block
0006  0010  #1J JMP  1M                    6034 ]
0007  0011        JMP  1M                  6034 |
0010  0012  #2J JMP  2M                    6047 | Indirect jumps
0011  0013        JMP  2M                  6047 |
0012  0014  #3J JMP  1C                    6062 |
0013  0015        JMP  1C                  6062 ]
      0016        @20
0020  0017  #1S RSW                        0516 ]
0021  0020        ADM                      1140 | Increment start of next block
0022  0021        2                        0002 ]
0023  0022        ADA  i                   1120 ]
0024  0023        1L-1S+1                  0101 ] Add length of LPFROG
0025  0024        ADA  i                   1120 ]
0026  0025        5777                     5777 | Check to see if next block will
0027  0026        APO                      0451 | exceed 1777
0030  0027        JMP  1J                  6006 ] Will not exceed. Jump to 1M
0031  0030        ADA  i                   1120 ]
0032  0031        20                       0020 | Will exceed. Relocate to
0033  0032        STC  2                   4002 | 20 plus residue of above
0034  0033  #1M LDA                        1000 | calculation
0035  0034        1                        0001 |
0036  0035        ADA  i                   1120 | Compute start of present block
0037  0036        7776                     7776 | minus 1
0040  0037        STC  4                   4004 ]
0041  0040        ADD  2                   2002 ]
0042  0041        ADA  i                   1120 | Compute start of next block
0043  0042        7776                     7776 | minus 1
0044  0043        STC  5                   4005 ]
0045  0044        SET  i 3                 0063 ] Set counter to - number of
0046  0045        JMP  1S-1L-1             7676 ] words in LPFROG
0047  0046  #2M LDA  i 4                   1024 ]
0050  0047        STA  i 5                 1065 ] Move LPFROG
0051  0050        XSK  i 3                 0223   More words in block ?
0052  0051        JMP  2J                  6010   YES. Jump to 2M, else do
0053  0052        LDA                      1000 ] check sum
0054  0053        1                        0001 |
0055  0054        ADA  i                   1120 | Compute start address of
0056  0055        7776                     7776 | present block minus 1
0057  0056        STC  4                   4004 ]
0060  0057        SET  i 3                 0063 ] Set counter to - number of
0061  0060        JMP  1S-1L-1             7676 ] words in LPFROG
0062  0061  #1C BCO  i 4                   1664   Form check sum
0063  0062        XSK  i 3                 0223   More words in block ?
0064  0063        JMP  3J                  6012   YES. Jump to 1C
0065  0064        SAE  i                   1460 ] NO. Check
0066  0065        7777                     7777 ]
0067  0066        HLT                      0000   Error halt. Incorrect checksum
0070  0067        LDA                      1000 ]
0071  0070        2                        0002 |
0072  0071        ADA  i                   1120 | Compute start address of next
0073  0072        7757                     7757 ] block minus 20
0074  0073        APO                      0451 ]
0075  0074        COM                      0017 | Make positive and store in TEMP
0076  0075        STC  3                   4003 ]
0077  0076        ADD  1J+1                2007 ]
0100  0077        ADD  3                   2003 ]
```

```
0101  0100          STC 1J          4006  [LEAP FROG
0102  0101          ADD 2J+1        2011
0103  0102          ADD 3           2003
0104  0103          STC 2J          4010  Change indirect jumps
0105  0104          ADD 3J+1        2013
0106  0105          ADD 3           2003
0107  0106          STC 3J          4012
0110  0107          LDA             1000
0111  0110          2               0002
0112  0111          STA             1040
0113  0112          1               0001  Make start address of next block
0114  0113          BSE i           1620  = start address of present block
0115  0114          JMP 0           6000
0116  0115          STC 3           4003  Jump to next block
0117  0116          JMP 3           6003
0120  0117    #1L   5730            5730  Checksum
```